


苹果笔记本维修交流群：325742634


SYNC MASTER=713 MLB		SYNC DATE=11/18/2011	
PAGE TITLE			
System Block Diagram			
 Apple Inc.	DRAWING NUMBER		SIZE
	051-9276		D
REVISION			
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**J11 POWER SYSTEM ARCHITECTURE**

The diagram illustrates the power system architecture, starting from the AC ADAPTER IN (J6900) and the DCIN (14.5V) input. The power flows through various regulators and components, including the DC-DC converter (U7000), LDOs (U7400, U7720, U7780, U7790), and the PMU (U4900). The system is controlled by the COUGAR-POINT (PCH) and the CPU (U1000). The diagram shows the power distribution to various components, including the SMC (U4900), the PMU (U4900), and the CPU (U1000). The power is regulated by various regulators, including the DC-DC converter (U7000), LDOs (U7400, U7720, U7780, U7790), and the PMU (U4900). The system is controlled by the COUGAR-POINT (PCH) and the CPU (U1000). The diagram shows the power distribution to various components, including the SMC (U4900), the PMU (U4900), and the CPU (U1000).

**Revision History**

REV	DESCRIPTION	DATE
1	Initial Release	11/18/2011
2	Update to J11 Power System Architecture	11/18/2011
3	Update to J11 Power System Architecture	11/18/2011
4	Update to J11 Power System Architecture	11/18/2011
5	Update to J11 Power System Architecture	11/18/2011
6	Update to J11 Power System Architecture	11/18/2011
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80	Update to J11 Power System Architecture	11/18/2011
81	Update to J11 Power System Architecture	11/18/2011
82	Update to J11 Power System Architecture	

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 Apple Inc.		Revision History	
		DRAWING NUMBER 051-9276	SIZE D
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		SHEET 3 OF 72	

BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
639-3469	PCBA,MLB,1.5GHZ,HY 4GB,J11	J11_CMNPTS,CPU:1.5GHZ,EEEE:DYKL,DDR3:HYNIX_4GB
639-3470	PCBA,MLB,1.5GHZ,SA 4GB,J11	J11_CMNPTS,CPU:1.5GHZ,EEEE:DYKH,DDR3:SAMSUNG_4GB
639-3473	PCBA,MLB,1.5GHZ,HY 8GB,J11	J11_CMNPTS,CPU:1.5GHZ,EEEE:DYKJ,DDR3:HYNIX_8GB
639-3659	PCBA,MLB,1.5GHZ,EL 8GB,J11	J11_CMNPTS,CPU:1.5GHZ,EEEE:FOVJ,DDR3:ELPIDA_8GB
639-3471	PCBA,MLB,1.7GHZ,HY 4GB,J11	J11_CMNPTS,CPU:1.7GHZ,EEEE:DYKJ,DDR3:HYNIX_4GB
639-3472	PCBA,MLB,1.7GHZ,SA 4GB,J11	J11_CMNPTS,CPU:1.7GHZ,EEEE:DYKF,DDR3:SAMSUNG_4GB
639-3775	PCBA,MLB,1.7GHZ,EL 4GB,J11	J11_CMNPTS,CPU:1.7GHZ,EEEE:F27J,DDR3:ELPIDA_4GB
639-3474	PCBA,MLB,1.7GHZ,HY 8GB,J11	J11_CMNPTS,CPU:1.7GHZ,EEEE:DYKJ,DDR3:HYNIX_8GB
639-3774	PCBA,MLB,1.7GHZ,SA 8GB,J11	J11_CMNPTS,CPU:1.7GHZ,EEEE:F27D,DDR3:SAMSUNG_8GB
639-3660	PCBA,MLB,1.7GHZ,EL 8GB,J11	J11_CMNPTS,CPU:1.7GHZ,EEEE:FOVJ,DDR3:ELPIDA_8GB
639-3776	PCBA,MLB,2.0GHZ,HY 4GB,J11	J11_CMNPTS,CPU:2.0GHZ,EEEE:F27K,DDR3:HYNIX_4GB
639-3778	PCBA,MLB,2.0GHZ,SA 4GB,J11	J11_CMNPTS,CPU:2.0GHZ,EEEE:F27G,DDR3:SAMSUNG_4GB
639-3780	PCBA,MLB,2.0GHZ,EL 4GB,J11	J11_CMNPTS,CPU:2.0GHZ,EEEE:F27H,DDR3:ELPIDA_4GB
639-3777	PCBA,MLB,2.0GHZ,HY 8GB,J11	J11_CMNPTS,CPU:2.0GHZ,EEEE:F27C,DDR3:HYNIX_8GB
639-3779	PCBA,MLB,2.0GHZ,SA 8GB,J11	J11_CMNPTS,CPU:2.0GHZ,EEEE:F27F,DDR3:SAMSUNG_8GB
639-3781	PCBA,MLB,2.0GHZ,EL 8GB,J11	J11_CMNPTS,CPU:2.0GHZ,EEEE:F279,DDR3:ELPIDA_8GB
085-3937	J11 MLB DEVELOPMENT BOM	J11_DEVEL-BMG
607-9089	CMN PTS,PCBA,MLB,J11	J11_CMNCHN
939-0479	PCBA,MLB,1.9GHZ,HY 4GB,J11	J11_CMNPTS,CPU:1.9GHZ,EEEE:DYKJ,DDR3:HYNIX_4GB

Bar Code Labels / EEEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
825-7670	1	LABEL,TEXT,MLB,K21/K78	[EEEE_DYKL]	CRITICAL	EEEE:DYKL
825-7670	1	LABEL,TEXT,MLB,K21/K78	[EEEE_DYKH]	CRITICAL	EEEE:DYKH
825-7670	1	LABEL,TEXT,MLB,K21/K78	[EEEE_DYKJ]	CRITICAL	EEEE:DYKJ
825-7670	1	LABEL,TEXT,MLB,K21/K78	[EEEE_DYKF]	CRITICAL	EEEE:DYKF
825-7670	1	LABEL,TEXT,MLB,K21/K78	[EEEE_DYKJ]	CRITICAL	EEEE:DYKJ
825-7670	1	LABEL,TEXT,MLB,K21/K78	[EEEE_DYKG]	CRITICAL	EEEE:DYKG
825-7670	1	LABEL,TEXT,MLB,K21/K78	[EEEE_FOVJ]	CRITICAL	EEEE:FOVJ
825-7670	1	LABEL,TEXT,MLB,K21/K78	[EEEE_FOV4]	CRITICAL	EEEE:FOV4
825-7670	1	LABEL,TEXT,MLB,K21/K78	[EEEE_F279]	CRITICAL	EEEE:F279
825-7670	1	LABEL,TEXT,MLB,K21/K78	[EEEE_F27C]	CRITICAL	EEEE:F27C
825-7670	1	LABEL,TEXT,MLB,K21/K78	[EEEE_F27D]	CRITICAL	EEEE:F27D
825-7670	1	LABEL,TEXT,MLB,K21/K78	[EEEE_F27F]	CRITICAL	EEEE:F27F
825-7670	1	LABEL,TEXT,MLB,K21/K78	[EEEE_F27G]	CRITICAL	EEEE:F27G
825-7670	1	LABEL,TEXT,MLB,K21/K78	[EEEE_F27H]	CRITICAL	EEEE:F27H
825-7670	1	LABEL,TEXT,MLB,K21/K78	[EEEE_F27J]	CRITICAL	EEEE:F27J
825-7670	1	LABEL,TEXT,MLB,K21/K78	[EEEE_F27K]	CRITICAL	EEEE:F27K

Sub-BOMs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
085-3937	1	J11 MLB DEVELOPMENT BOM	DEVEL	CRITICAL	DEVEL_BOM
607-9089	1	CMN PTS,PCBA,MLB,J11	CMNPTS	CRITICAL	J11_CMNPTS

SYNC MASTER=K21 MLB

SYNC DATE=11/16/2010

K78 BOM Variants

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Functional Test Points

J4001: AirPort / BT Connector

PUNC_TEST		
TRUE	PP3V3 WLAN F (Need 6 TPs)	36 41
TRUE	WIFI EVENT L	36 40 41
TRUE	PCIE AP R2D N	36 68
TRUE	PCIE AP R2D P	36 68
TRUE	PCIE CLK100M AP N	16 36 68
TRUE	PCIE CLK100M AP P	16 36 68
TRUE	USB BT CONN P	36 67
TRUE	USB BT CONN N	36 67
TRUE	PCIE AP D2R P	16 36 68
TRUE	PCIE AP D2R N	16 36 68
TRUE	PCIE WAKE L	37 36
TRUE	AP RESET CONN L	36
TRUE	AP CLKREQ O L	36
TRUE	PP3V3 SIRS4 BT F	36
(Need to add 8 GND TPs)		

J4501: SATA SSD Connector

PUNC_TEST		
TRUE	PP3V3 S0 SSD FLT (Need 5 TPs)	37
TRUE	SATA SSD D2R P	37 67
TRUE	SATA SSD D2R N	37 67
TRUE	SATA SSD R2D N	37 67
TRUE	SATA SSD R2D P	37 67
TRUE	SMC OOB1 RX L	37 40
TRUE	SMC OOB1 TX L	37 40 41
TRUE	PCIE SSD D2R N<1>	8 37 65
TRUE	PCIE SSD D2R P<1>	8 37 65
TRUE	PCIE SSD R2D N<1>	37 65
TRUE	PCIE SSD R2D P<1>	37 65
TRUE	PCIE CLK100M SSD N	16 37 65
TRUE	PCIE CLK100M SSD P	16 37 65
TRUE	SSD CLKREQ L	16 37
TRUE	SSD RESET L	26 37
TRUE	SATA PCIE SEL	37
TRUE	SSD P3V3S0 EN	37
(Need to add 6 GND TPs)		

J4700: LIO Connector

PUNC_TEST		
TRUE	=PP3V42 G3H ONEWIRE	7 39
TRUE	=PP3V3 S0 AUDIO	7 39
TRUE	=PP3V3R1V5 S0 AUDIO	7 39
TRUE	SYS ONEWIRE	39 40
TRUE	SMC BC ACOK	38 39 41
TRUE	=USB PWR EN	38 39 61
TRUE	=I2C LIO SDA	39 43
TRUE	=I2C LIO SCL	39 43
TRUE	=I2C MIKEY SCL	39 43
TRUE	=I2C MIKEY SDA	39 43
TRUE	AUD IPHS SWITCH EN	25 39
TRUE	AUD IP PERIPHERAL DET	18 39
TRUE	AUD I2C INT L	18 39
TRUE	AUD GPIO 3	39 50
TRUE	SPKRAMP INR N	39 50 71
TRUE	SPKRAMP INR P	39 50 71
TRUE	USB EXTB N	24 39 67
TRUE	USB EXTB P	24 39 67
TRUE	USB CAMERA N	18 39 67
TRUE	USB CAMERA P	18 39 67
TRUE	HDA SDOUT	16 39 68
TRUE	HDA BIT CLK	16 39 68
TRUE	HDA SDIN0	16 39 68
TRUE	USB EXTB OC L	23 39
TRUE	HDA RST L	16 39 68
TRUE	HDA SYNC	16 39 68
TRUE	USB3 EXTB RX RC N	39 67
TRUE	USB3 EXTB RX RC P	39 67
TRUE	USB3 EXTB TX C P	39 67
TRUE	USB3 EXTB TX C N	39 67
(Need to add 5 GND TPs)		

J5100: LPC+SPI Connector

PUNC_TEST		
TRUE	=PP3V3 S5 LPCPLUS	7 42
TRUE	=PP5V S0 LPCPLUS	7 42
TRUE	LPC AD<3..0>	16 40 42 68
TRUE	SPI ALT MOSI	42
TRUE	SPI ALT MISO	42
TRUE	LPC FRAME L	16 40 42 68
TRUE	PM CLKRUN L	17 42
TRUE	SMC TMS	40 41 42
TRUE	LPCPLUS RESET L	25 42 68
TRUE	SMC TDO	40 41 42
TRUE	TP SMC TRST L	42
TRUE	TP SMC MD1	42
TRUE	SMC TX L	40 41 42
TRUE	LPC CLK33M LPCPLUS	25 42 68
TRUE	SPIROM USE MLB	19 42 68
TRUE	SPI ALT CLK	42
TRUE	SPI ALT CS L	42
TRUE	LPC SERIRO	16 40 42
TRUE	LPC PMRDWN L	17 25 40 42
TRUE	SMC TDI	40 41 42
TRUE	SMC TCK	40 41 42
TRUE	SMC RESET L	40 41 42 52
TRUE	SMC ROMBOOT	41 42
TRUE	SMC RX L	40 41 42
TRUE	LPCPLUS GPIO	19 42
(Need to add 6 GND TPs)		

J5600: Fan Connector

PUNC_TEST		
TRUE	=PP5V S0 FAN	7 47
TRUE	FAN RT TACH	47
TRUE	FAN RT PWM	47
(Need to add 1 GND TP)		

J5700: IPD Flex Connector

PUNC_TEST		
TRUE	SMC PME S4 WAKE L	40 41 48
TRUE	PP5V TPAD FILT	48
TRUE	=PP3V42 G3H TPAD	7 48
TRUE	PP3V3 TPAD CONN	48
TRUE	USB TPAD P	48 67
TRUE	USB TPAD N	48 67
TRUE	=I2C TPAD SDA	43 48
TRUE	=I2C TPAD SCL	43 48
TRUE	SMC ONOFF L	40 41 48
TRUE	SMC LID	40 41 48 51
TRUE	SMC TPAD RST L	41 48
(Need to add 5 GND TPs)		

J6900: DC-In Connector

PUNC_TEST		

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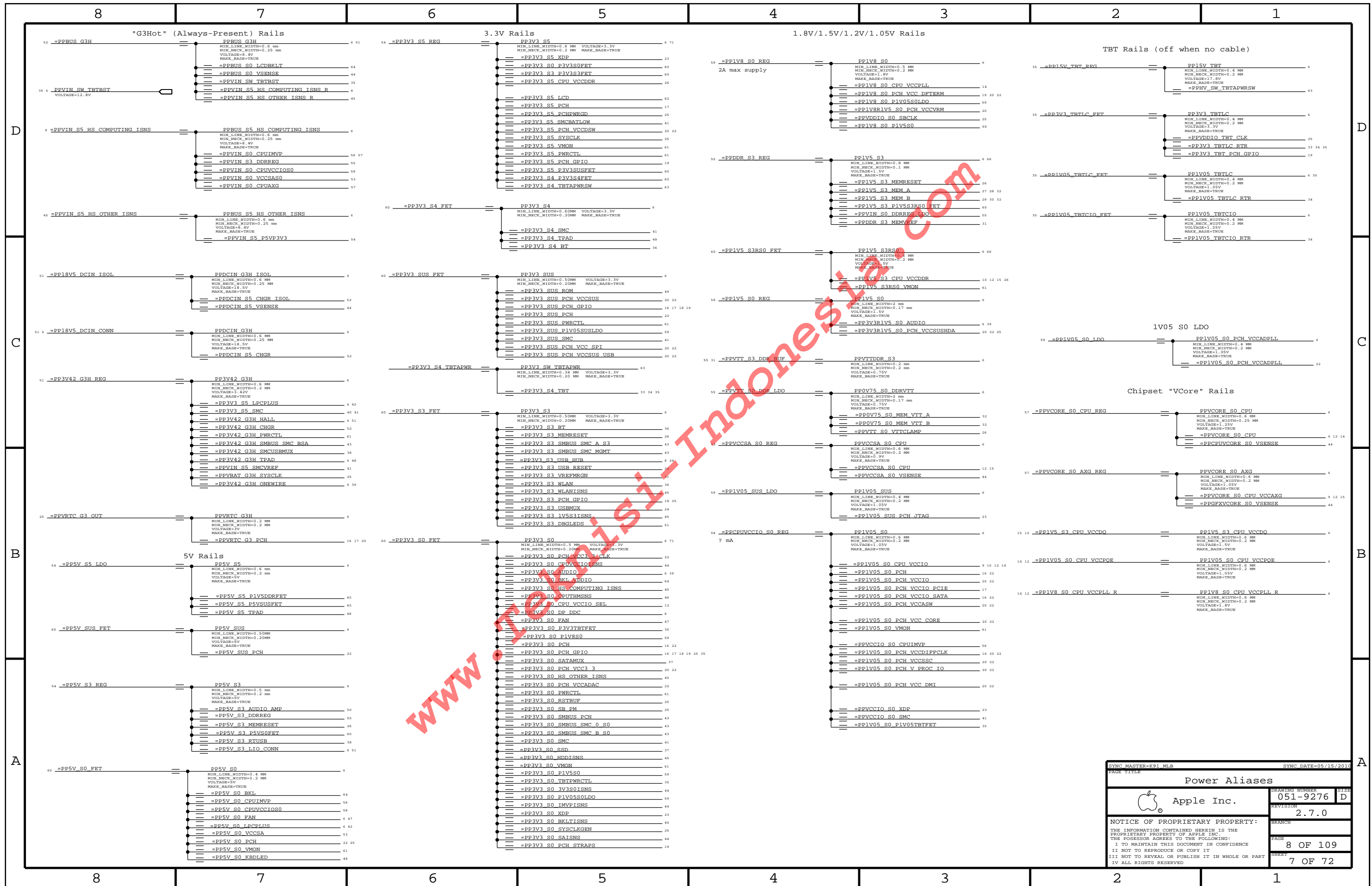
7 51
PPBUS_G3H
7
PPVIN_SM TBTBST
7 35
PPBUS_S5 HS COMPUTING ISNS
7
PPDCIN_G3H
7
PP3V42_G3H
7
PPVRTC_G3H
7
PP5V_S5
7
PP5V_SUS
7
PP3V3_S5
7 71
PP3V3_SUS
7
PP3V3_S3
7
PP1V8_S0
7
PP3V3_S0
7 71
PP1V5_S3
7 66
PP1V5_S3RS0
7 66
PP1V5_S0
PP1V05_S0
PPVTTDDR_S3
7
PPQV75_S0 DDRVTT
7
PPVCCSA_S0 CPU
7
PP1V05_SUS
7
PP15V_TBT
7
PP3V3_TBTLG
7 (Need to add 27 GND 1
PP1V05_TBTLG
7 35
PP1V05_S0 PCH VCCADPLL
7
PPVCORE_S0 CPU
7
PPVCORE_S0 AXG
7
PP1V5_S3 CPU VCCDQ
7
PP1V05_S0 CPU VCCPOE
7
PP1V8_S0 CPU VCCPLL_R
7
PP1V05_TBTCIO
7
PPBUS_S5 HS OTHER ISNS
7
PPDCIN_G3H ISOL
7
PP5V_S3
7
PP5V_S0
7
PP3V3_S4
7

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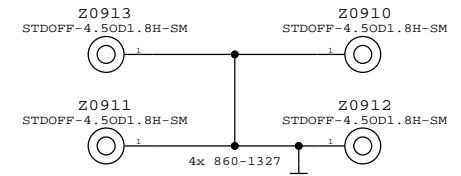
POWER SIGNALS			
<b>16A1</b>	_____	VCCCSAS0_SREF	53
<b>16A2</b>	_____	VCCCSAS0_SET1_B	53
<b>16A3</b>	_____	VCCCSAS0_SET0	53
<b>16A4</b>	_____	VCCCSAS0_SET1	53
NC_TEST			
17	TP_CRT_IG_BLUE	=====	NC_CRT_IG_BLUE
		=====	NAME_SASX-TRUE
17	TP_CRT_IG_GREEN	=====	NC_CRT_IG_GREEN
		=====	NAME_SASX-TRUE
17	TP_CRT_IG_RED	=====	NC_CRT_IG_RED
		=====	NAME_SASX-TRUE
17	TP_CRT_IG_DDC_CLK	=====	NC_CRT_IG_DDC_CLK
		=====	NAME_SASX-TRUE
17	TP_CRT_IG_DDC_DATA	=====	NC_CRT_IG_DDC_DATA
		=====	NAME_SASX-TRUE
17	TP_CRT_IG_HVSNV'	=====	NC_CRT_IG_HVSNV'
		=====	NAME_SASX-TRUE
17	TP_CRT_IG_VSNV'	=====	NC_CRT_IG_VSNV'
		=====	NAME_SASX-TRUE
	TP_LVDS_IG_CTRL0_CLK	=====	NC_LVDS_IG_CTRL0_CLK
		=====	NAME_SASX-TRUE
	TP_LVDS_IG_CTRL0_DATA	=====	NC_LVDS_IG_CTRL0_DATA
		=====	NAME_SASX-TRUE
	TP_FCH_LVDS_VBG0	=====	NC_FCH_LVDS_VBG0
		=====	NAME

14	TP_PCIE_CLK100M_F04	=====	NAME	NC_PCIE_CLK100M_F04N
		=====	NAME_BASE-TRUE	
16	TP_PCIE_CLK100M_F04P	=====	NAME	NC_PCIE_CLK100M_F04P
		=====	NAME_BASE-TRUE	
	TP_PCIE_CLK100M_F05N	=====	NAME	NC_PCIE_CLK100M_F05N
		=====	NAME_BASE-TRUE	
	TP_PCIE_CLK100M_F05P	=====	NAME	NC_PCIE_CLK100M_F05P
		=====	NAME_BASE-TRUE	
	TP_PCIE_CLK100M_F06N	=====	NAME	NC_PCIE_CLK100M_F06N
		=====	NAME_BASE-TRUE	
	TP_PCIE_CLK100M_F06P	=====	NAME	NC_PCIE_CLK100M_F06P
		=====	NAME_BASE-TRUE	
	TP_PCIE_CLK100M_F07N	=====	NAME	NC_PCIE_CLK100M_F07N
		=====	NAME_BASE-TRUE	
	TP_PCIE_CLK100M_F07P	=====	NAME	NC_PCIE_CLK100M_F07P
		=====	NAME_BASE-TRUE	
	TP_PSOC_P1_3	=====	NAME	NC_PSOC_P1_3
		=====	NAME_BASE-TRUE	
	TP_SATA_B_D28N	=====	NAME	NC_SATA_B_D28N
		=====	NAME_BASE-TRUE	
	TP_SATA_B_D28P	=====	NAME	NC_SATA_B_D28P
		=====	NAME_BASE-TRUE	
	TP_SATA_B_R2D_CN	=====	NAME	NC_SATA_B_R2D_CN
		=====	NAME_BASE-TRUE	
	TP_SATA_B_R2D_CP	=====	NAME	NC_SATA_B_R2D_CP
		=====	NAME_BASE-TRUE	
	TP_SATA_D_D28N	=====	NAME	NC_SATA_D_D28N
		=====	NAME_BASE-TRUE	
16	TP_SATA_D_D28P	=====	NAME	NC_SATA_D_D28P
		=====	NAME_BASE-TRUE	
	TP_SATA_D_R2D_CN	=====	NAME	NC_SATA_D_R2D_CN
		=====	NAME_BASE-TRUE	
	TP_SATA_E_R2D_CP	=====	NAME	NC_SATA_E_R2D_CP
		=====	NAME_BASE-TRUE	
	TP_SATA_E_D28N	=====	NAME	NC_SATA_E_D28N
		=====	NAME_BASE-TRUE	
	TP_SATA_E_D28P	=====	NAME	NC_SATA_E_D28P
		=====	NAME_BASE-TRUE	
	TP_SATA_E_R2D_CN	=====	NAME	NC_SATA_E_R2D_CN
		=====	NAME_BASE-TRUE	
	TP_SATA_E_R2D_CP	=====	NAME	NC_SATA_E_R2D_CP
		=====	NAME_BASE-TRUE	
	TP_SATA_F_D28N	=====	NAME	NC_SATA_F_D28N
		=====	NAME_BASE-TRUE	
	TP_SATA_F_D28P	=====	NAME	NC_SATA_F_D28P
		=====	NAME_BASE-TRUE	
	TP_SATA_F_R2D_CN	=====	NAME	NC_SATA_F_R2D_CN
		=====	NAME_BASE-TRUE	
	TP_SATA_F_R2D_CP	=====	NAME	NC_SATA_F_R2D_CP
		=====	NAME_BASE-TRUE	

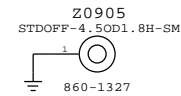
8	TP LVDS IG B CLKN	---	TRUE	NC LVDS IG B CLKN
		---	MAKE_BASE=TRUE	
8	TP LVDS IG B CLKP	---	TRUE	NC LVDS IG B CLKP
		---	MAKE_BASE=TRUE	
	TP LVDS IG BKL PWM	---	TRUE	NC LVDS IG BKL PWM
		---	MAKE_BASE=TRUE	



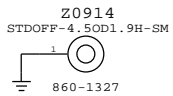
CPU Heat Sink Mounting Bosses



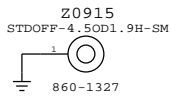
Fan Boss



X21 Boss

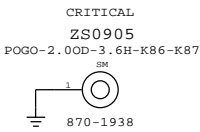


SSD Boss

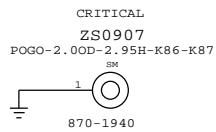


EMI I/O Pogo Pins

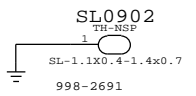
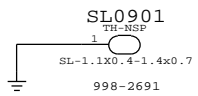
DisplayPort Pogo



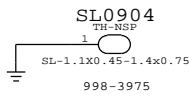
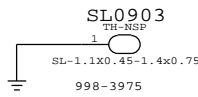
USB/SD Card Pogo



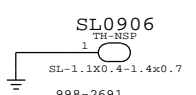
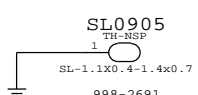
Can Slots



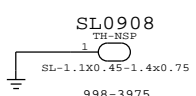
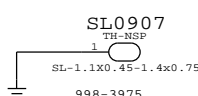
2x MDP connector



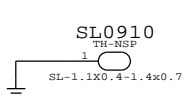
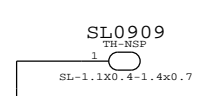
2x USB connector



2x TBT pin diodes

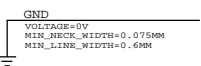


2x TBT chip



2x CPU Vcore

Digital Ground



CPU signals

26	MEMVTT EN	==	DDRVT EN	26	55
68	33	DP TBTSNK0 AUXCH C P	==	DPA IG AUX CH P	17
68	33	DP TBTSNK0 AUXCH C N	==	DPA IG AUX CH N	17
16	16	PCIE CLK100M ENET N	==	NC PCIE CLK100M ENETN	
16	16	PCIE CLK100M ENET P	==	NC PCIE CLK100M ENETP	
16	16	PCIE EXCARD D2R N	==	NC PCIE EXCARD D2RN	
16	16	PCIE EXCARD D2R P	==	NC PCIE EXCARD D2RP	
16	16	PCIE EXCARD R2D C N	==	NC PCIE EXCARD R2D CN	
16	16	PCIE EXCARD R2D C P	==	NC PCIE EXCARD R2D CP	
16	16	PCIE CLK100M EXCARD N	==	NC PCIE CLK100M EXCARDN	
16	16	PCIE CLK100M EXCARD P	==	NC PCIE CLK100M EXCARDP	

68	16	PEG CLK100M P	==	NC PEG CLK100MP	
68	16	PEG CLK100M N	==	NC PEG CLK100MN	
16	TP	PCH CLKOUT DPH	==	DP LL REF CLK N	10
16	TP	PCH CLKOUT DPP	==	DP LL REF CLK P	10
66	11	MEM A CLK P<1>	==	TP MEM A CLKP<1>	
66	11	MEM A CLK N<1>	==	TP MEM A CLKN<1>	
66	11	MEM B CLK P<1>	==	TP MEM B CLKP<1>	
66	11	MEM B CLK N<1>	==	TP MEM B CLKN<1>	

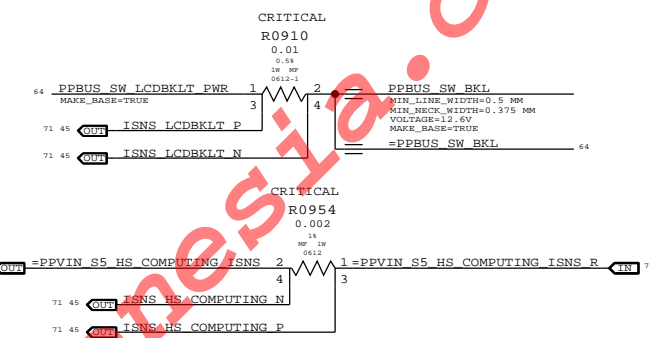
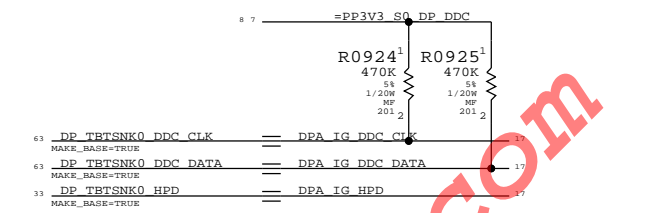
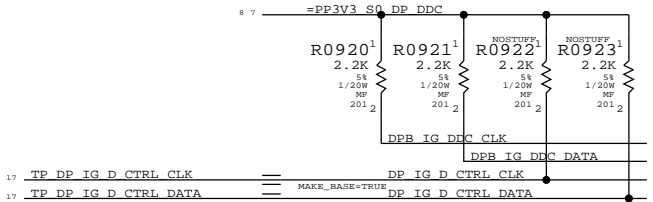
18	USB EXT C P	==	NC USB EXTCP	
18	USB EXT C N	==	NC USB EXTCN	
18	USB3 EXT C RX P	==	NC USB3 EXT C RXP	
18	USB3 EXT C RX N	==	NC USB3 EXT C RXN	
18	USB3 EXT C TX P	==	NC USB3 EXT C TXP	
18	USB3 EXT C TX N	==	NC USB3 EXT C TXN	
18	USB3 EXT D RX P	==	NC USB3 EXT D RXP	
18	USB3 EXT D RX N	==	NC USB3 EXT D RXN	
18	USB3 EXT D TX P	==	NC USB3 EXT D TXP	
18	USB3 EXT D TX N	==	NC USB3 EXT D TXN	
18	USB EXT D EHCI P	==	NC USB EXT D EHCIP	
18	USB EXT D EHCI N	==	NC USB EXT D EHCIN	

	TBT B R2D C P<0>	==	NC TBT B R2D CP<0>	
		MAKE_BASE=TRUE		
69 33	TBT B R2D C N<0>	==	NC TBT B R2D CN<0>	
		MAKE_BASE=TRUE		
69 33	TBT B R2D C P<1>	==	NC TBT B R2D CP<1>	
		MAKE_BASE=TRUE		
69 33	TBT B R2D C N<1>	==	NC TBT B R2D CN<1>	
		MAKE_BASE=TRUE		
69 33	TBT B D2R P<0>	==	NC TBT B D2RP<0>	
		MAKE_BASE=TRUE		
69 33	TBT B D2R N<0>	==	NC TBT B D2RN<0>	
		MAKE_BASE=TRUE		
69 33	TBT B D2R P<1>	==	NC TBT B D2RP<1>	
		MAKE_BASE=TRUE		
69 33	TBT B D2R N<1>	==	NC TBT B D2RN<1>	
		MAKE_BASE=TRUE		
33	TBT B LSTX	==	NC TBT B LSTX	
		MAKE_BASE=TRUE		

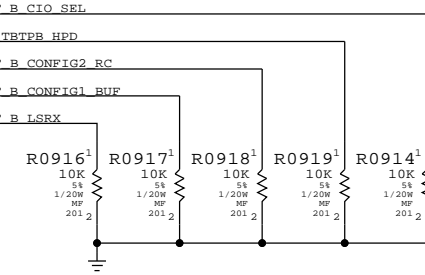
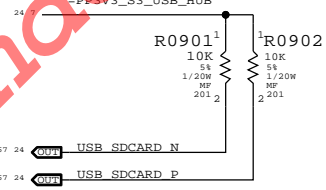
69	33	DP TBTTP ML C P<1>	==	NC DP TBTTP ML CP<1>	
69	33	DP TBTTP ML C N<1>	==	NC DP TBTTP ML CN<1>	
69	33	DP TBTTP ML C P<3>	==	NC DP TBTTP ML CP<3>	
69	33	DP TBTTP ML C N<3>	==	NC DP TBTTP ML CN<3>	

16	PCIE CLK100M FW N	==	NC PCIE CLK100M FWN	
16	PCIE CLK100M FW P	==	NC PCIE CLK100M FWP	
9	=PEG D2R P<1..0>	==	PCIE SSD D2R P<1..0>	6
9	=PEG D2R N<1..0>	==	PCIE SSD D2R N<1..0>	6
9	=PEG R2D C P<1..0>	==	PCIE SSD R2D C P<1..0>	37
9	=PEG R2D C N<1..0>	==	PCIE SSD R2D C N<1..0>	37

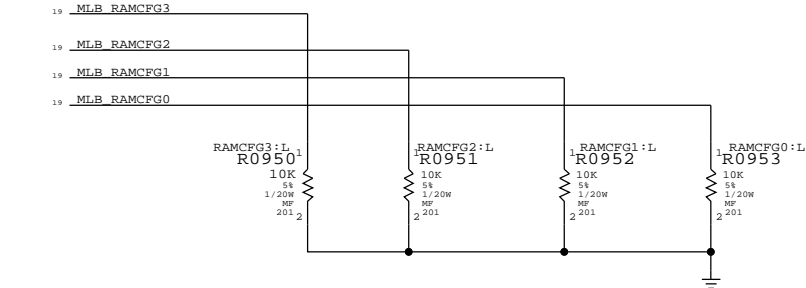
16	PCIE ENET D2R N	==	NC PCIE ENET D2RN	
16	PCIE ENET D2R P	==	NC PCIE ENET D2RP	
16	PCIE ENET R2D C N	==	NC PCIE ENET R2D CN	
16	PCIE ENET R2D C P	==	NC PCIE ENET R2D CP	
16	PCIE FW D2R N	==	NC PCIE FW D2RN	
16	PCIE FW D2R P	==	NC PCIE FW D2RP	
16	PCIE FW R2D C N	==	NC PCIE FW R2D CN	
16	PCIE FW R2D C P	==	NC PCIE FW R2D CP	



UNUSED SDCARD USB Aliases



23	19	XDP DD3 PCH GPIO49 ENET LOW PWR PCH	==	ENET LOW PWR PCH	19
23	16	XDP DC3 PCH GPIO19 SATARDRV EN	==	SATARDRV EN	16



TBT DP Ports

17	DPB IG HPD	==	DP TBTSNK1 HPD	33
17	TP DP IG C MLP<3..0>	==	MAKE_BASE=TRUE DP TBTSNK1 ML C P<3..0>	33 68
17	TP DP IG C MLN<3..0>	==	MAKE_BASE=TRUE DP TBTSNK1 ML C N<3..0>	33 68
17	DPB IG AUX CH P	==	MAKE_BASE=TRUE DP TBTSNK1 AUXCH C P	33 68
17	DPB IG AUX CH N	==	MAKE_BASE=TRUE DP TBTSNK1 AUXCH C N	33 68
17	TP DP IG D HPD	==	DP IG D HPD	
		==	MAKE_BASE=TRUE	
69	33 DP TBTBP AUXCH C P	==	NC DP TBTBP AUXCH CP	
69	33 DP TBTBP AUXCH C N	==	MAKE_BASE=TRUE NC DP TBTBP AUXCH CN	
		==	MAKE_BASE=TRUE	
17	TP DP IG B MLP<3..0>	==	DP TBTSNK0 ML C P<3..0>	33 68
17	TP DP IG B MLN<3..0>	==	MAKE_BASE=TRUE DP TBTSNK0 ML C N<3..0>	33 68
		==	MAKE_BASE=TRUE	

R0909100R

1/20W 80F 201

16	NC PCIE 5 R2D CP	==	PCIE TBT R2D C P<0>	33
16	NC PCIE 6 R2D CP	==	PCIE TBT R2D C P<1>	33
16	NC PCIE 7 R2D CP	==	PCIE TBT R2D C P<2>	33
16	NC PCIE 8 R2D CP	==	PCIE TBT R2D C P<3>	33
16	NC PCIE 5 R2D CN	==	PCIE TBT R2D C N<0>	33
16	NC PCIE 6 R2D CN	==	PCIE TBT R2D C N<1>	33
16	NC PCIE 7 R2D CN	==	PCIE TBT R2D C N<2>	33
16	NC PCIE 8 R2D CN	==	PCIE TBT R2D C N<3>	33
16	NC PCIE 5 D2RP	==	PCIE TBT D2R P<0>	33
16	NC PCIE 6 D2RP	==	PCIE TBT D2R P<1>	33
16	NC PCIE 7 D2RP	==	PCIE TBT D2R P<2>	33
16	NC PCIE 8 D2RP	==	PCIE TBT D2R P<3>	33
16	NC PCIE 5 D2RN	==	PCIE TBT D2R N<0>	33
16	NC PCIE 6 D2RN	==	PCIE TBT D2R N<1>	33
16	NC PCIE 7 D2RN	==	PCIE TBT D2R N<2>	33
16	NC PCIE 8 D2RN	==	PCIE TBT D2R N<3>	33

LVDS Aliases

6	TP LVDS IG B CLKP	==	LVDS IG B CLK P	
6	TP LVDS IG B CLKN	==	LVDS IG B CLK N	
6	NC LVDS IG B DATAP<0..3>	==	LVDS IG B DATA P<0..3>	
6	NC LVDS IG B DATAN<0..3>	==	LVDS IG B DATA N<0..3>	
6	NC LVDS IG A DATAP<3>	==	LVDS IG A DATA P<3>	
6	NC LVDS IG A DATAN<3>	==	LVDS IG A DATA N<3>	
64	LCD BKLT PWM	==	LVDS IG BKL PWM	17
64	LCD IG PWR EN	==	LVDS IG PANEL PWR	17
64	LCD BKLT EN	==	LVDS IG BKL ON	17

SATA Aliases

Unused SATA ODD Signals

16	NC SATA ODD R2D C P	==	NC SATA ODD R2DCP	
16	NC SATA ODD R2D C N	==	NC SATA ODD R2DCN	
16	NC SATA ODD D2R P	==	NC SATA ODD D2RP	
16	NC SATA ODD D2R N	==	NC SATA ODD D2RN	

SMC Aliases

Unused SMC Signals

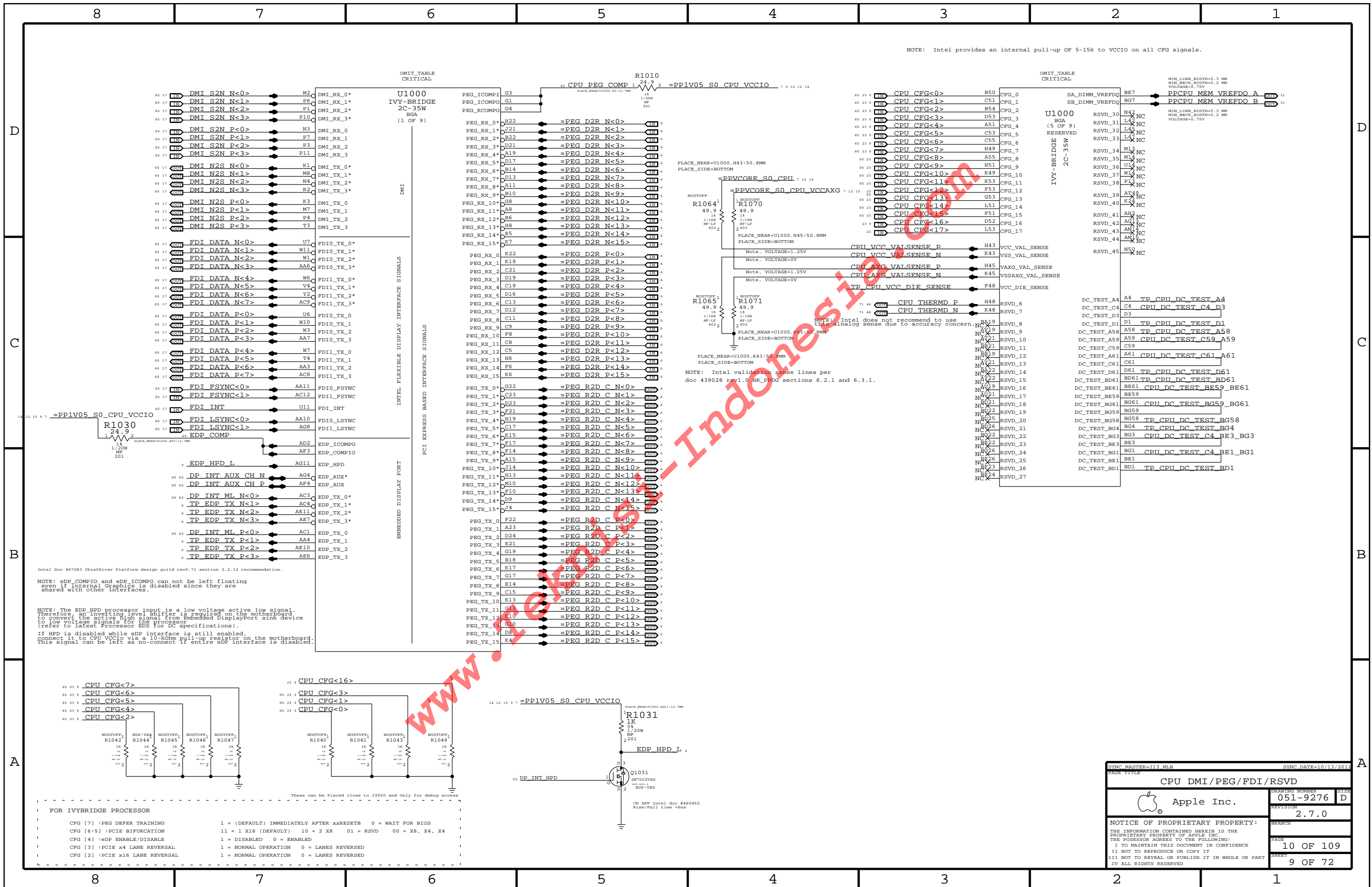
40	NC SMC SYS LED	==	NC SMC SYS LED	
40	IR RX OUT RC	==	NC IR RX OUT RC	

Unused PGOOD signal

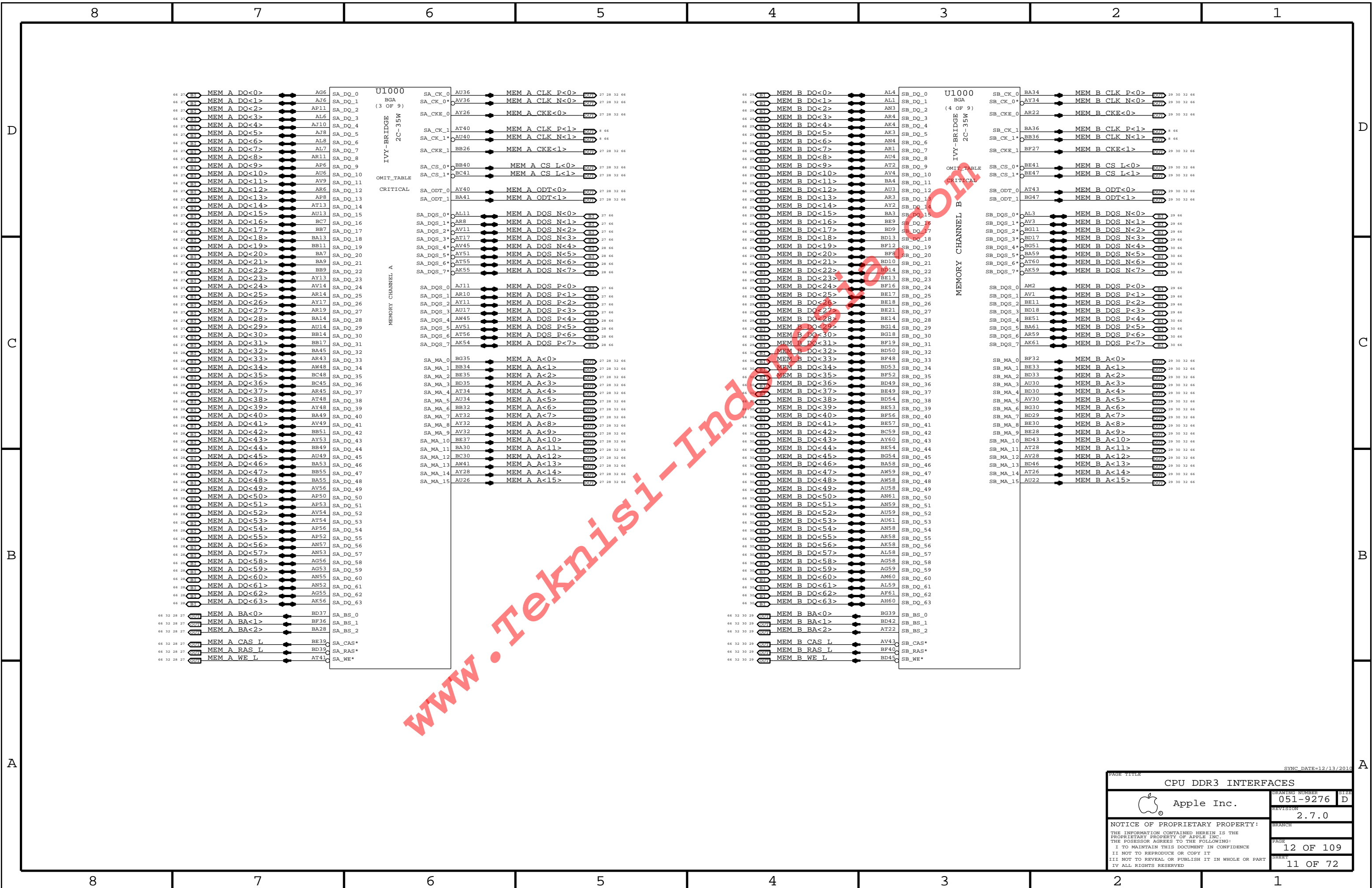
TP	P1V5S3RS0 RAMP DONE	==	P1V5S3RS0 RAMP DONE	INT	50
TP	DDRREG PGOOD	==	DDRREG PGOOD	INT	55

SYNC MASTER=K91 MLB		SYNC DATE=05/15/2010	
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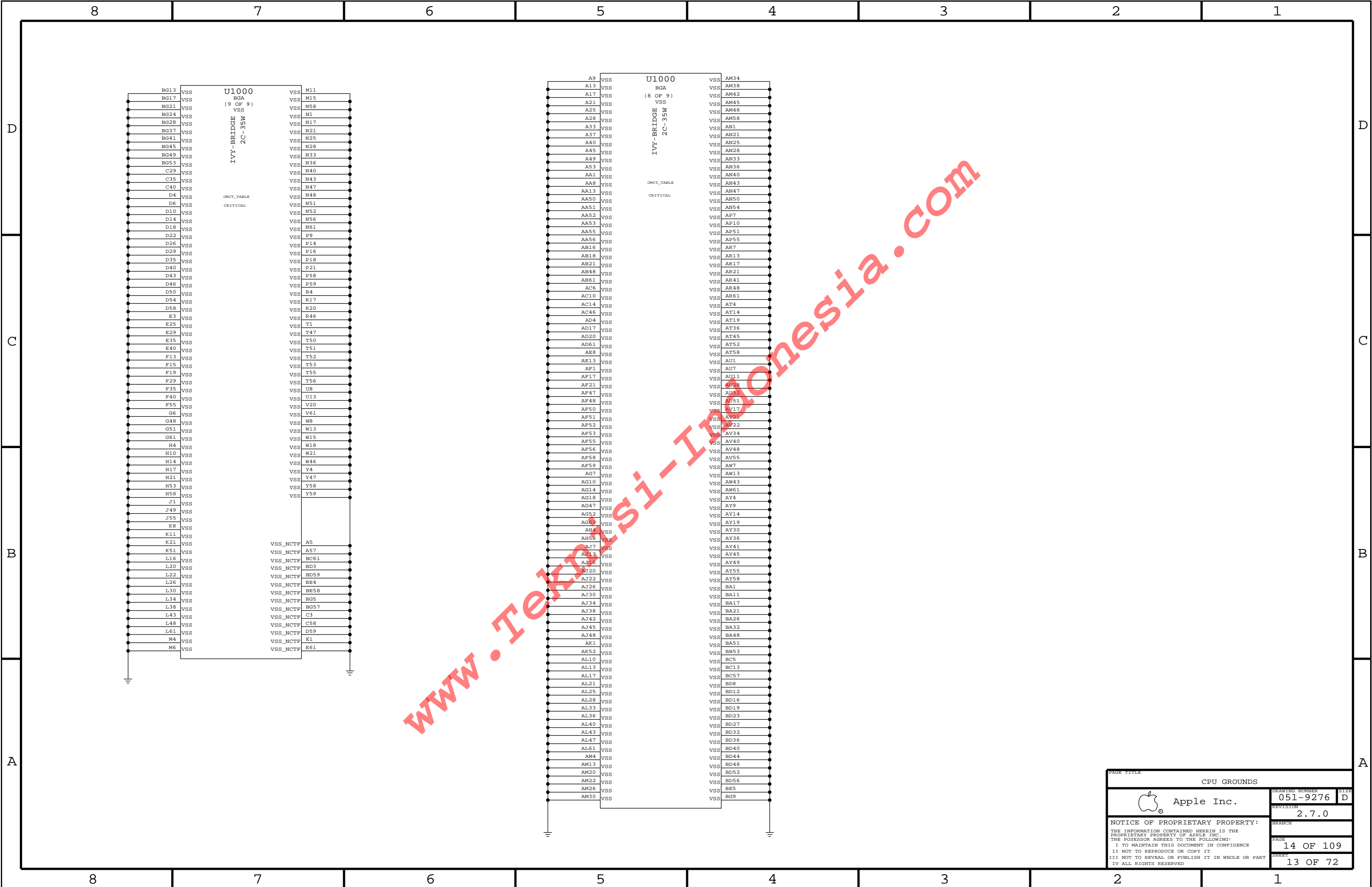




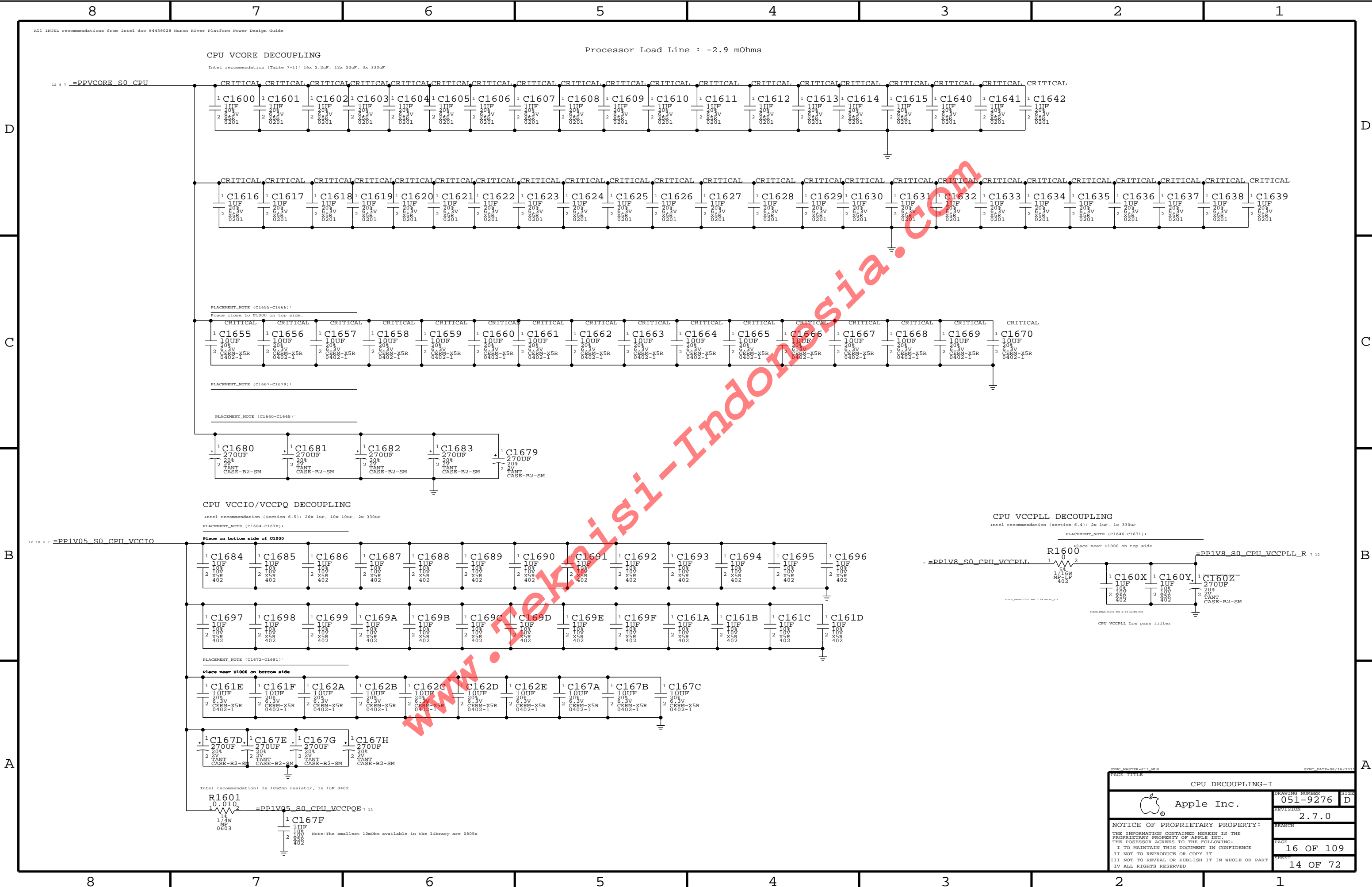





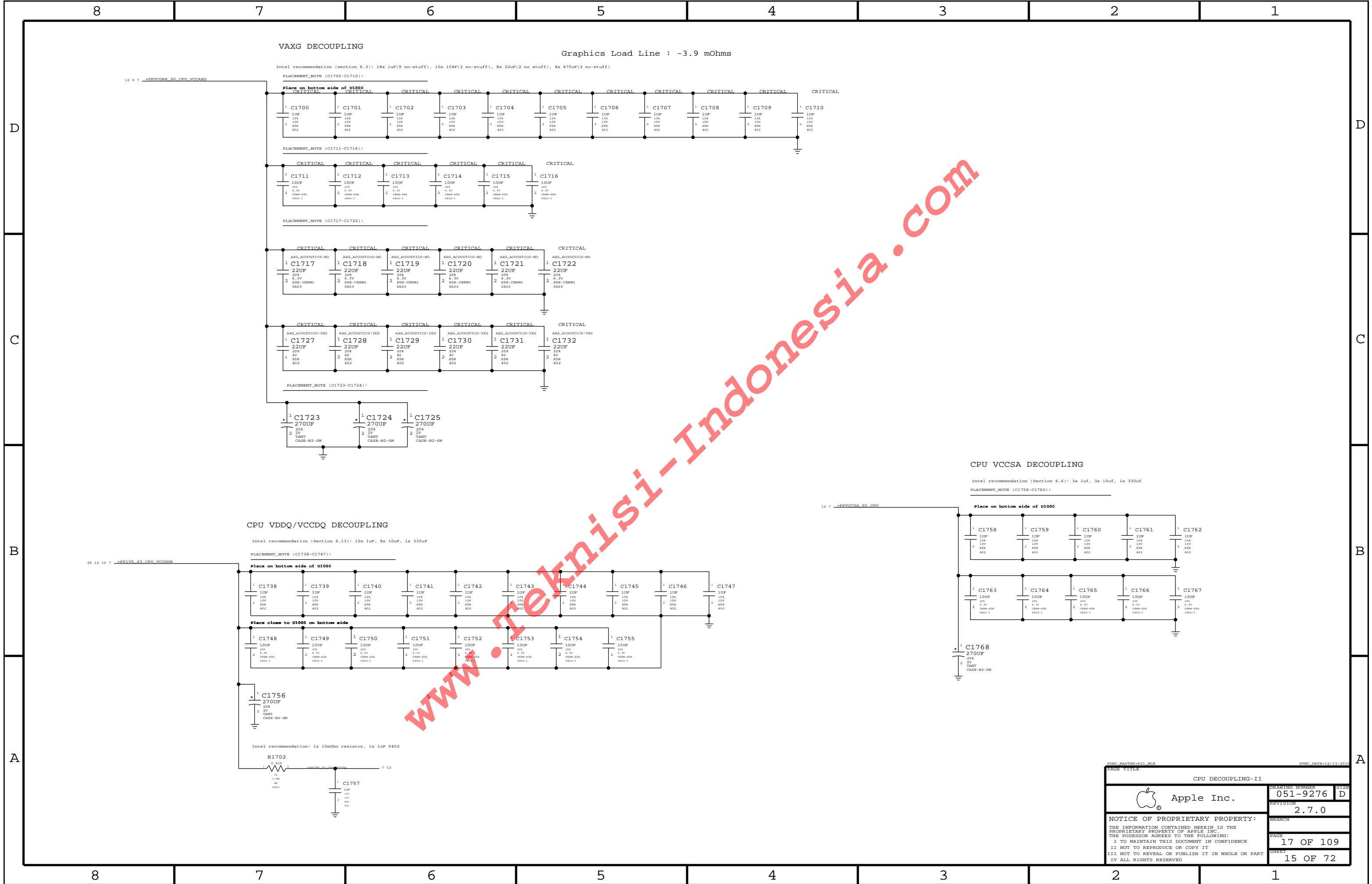


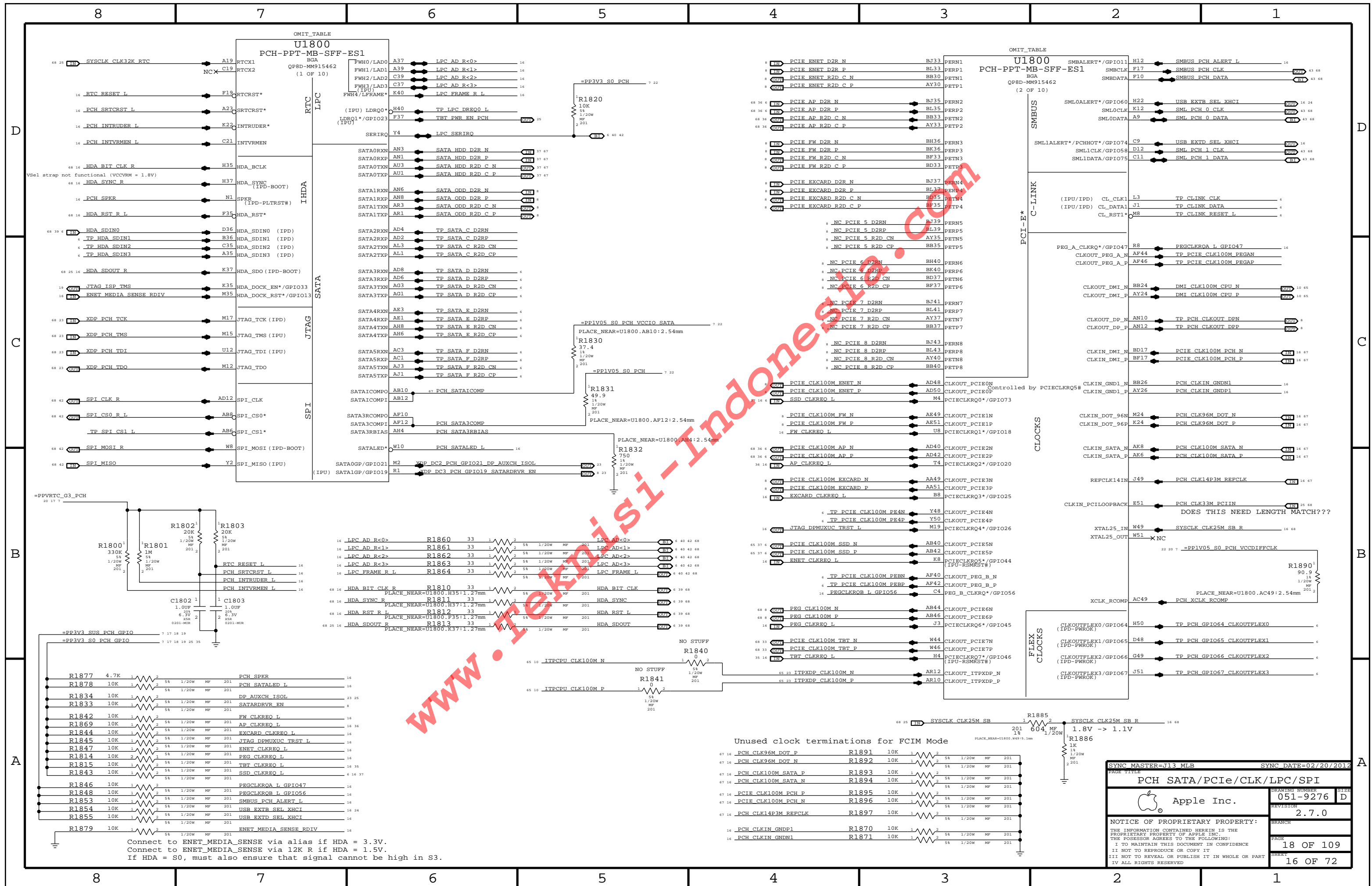


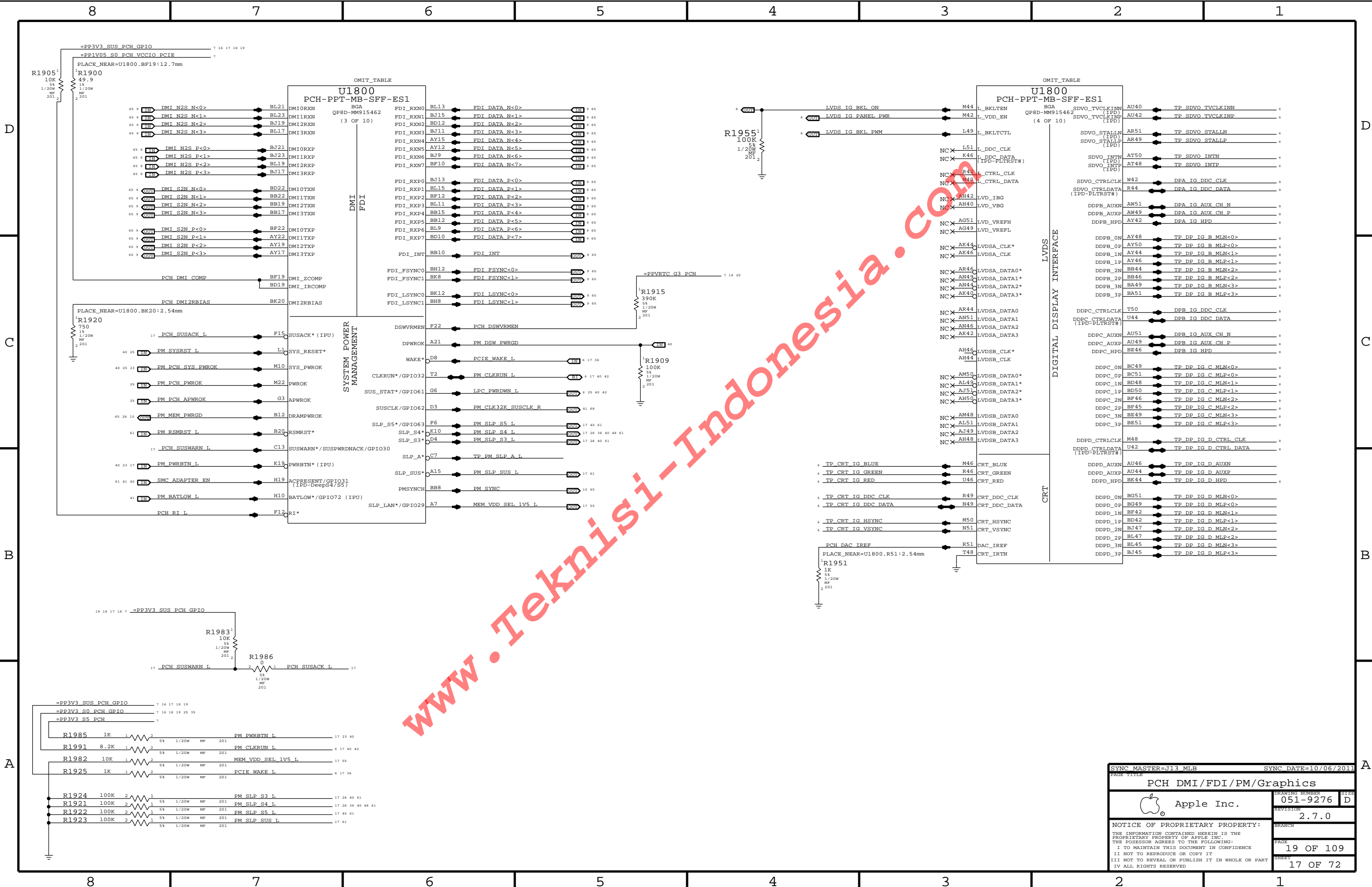


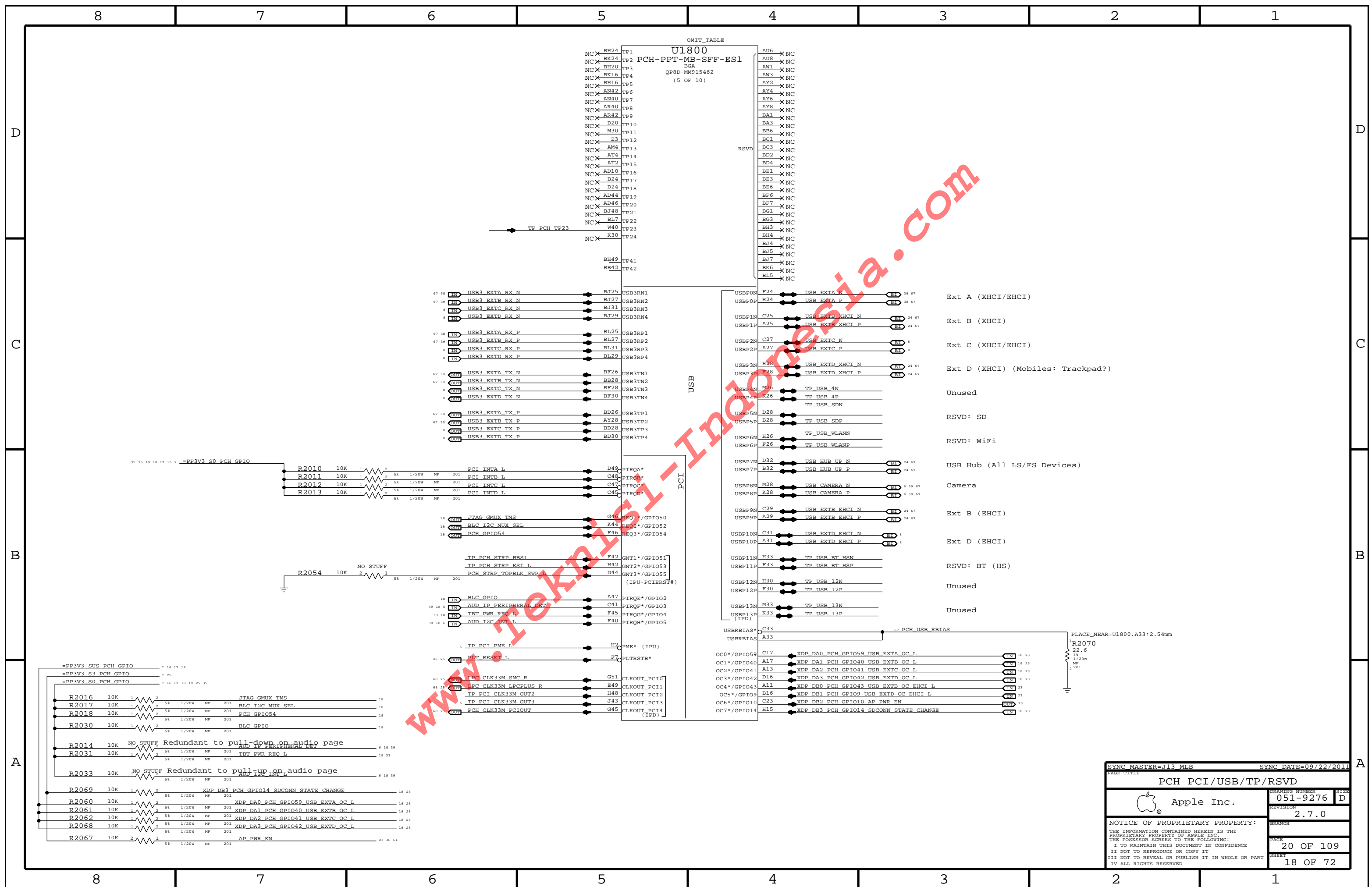


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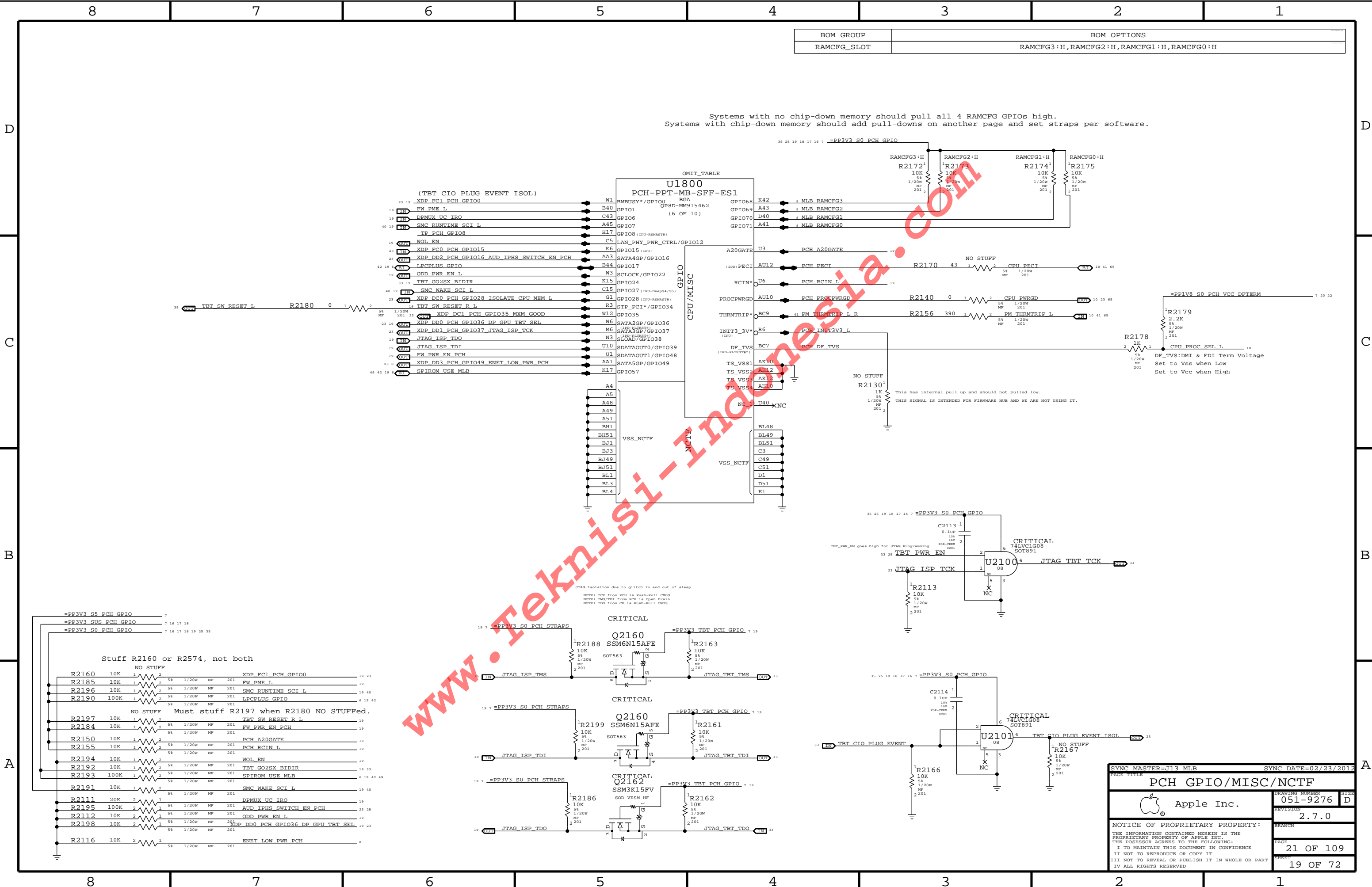












Systems with no chip-down memory should pull all 4 RAMCFG GPIOs high.  
Systems with chip-down memory should add pull-downs on another page and set straps per software.

BOM GROUP	BOM OPTIONS
RAMCFG_SLOT	RAMCFG3:H, RAMCFG2:H, RAMCFG1:H, RAMCFG0:H

OMIT_TABLE
U1800 PCH-PPT-MB-SFF-ES1

SYNC MASTER=J13 MLB

SYNC DATE=02/23/2012

PCH GPIO/MISC/NCTF

Apple Inc.

051-9276

2.7.0

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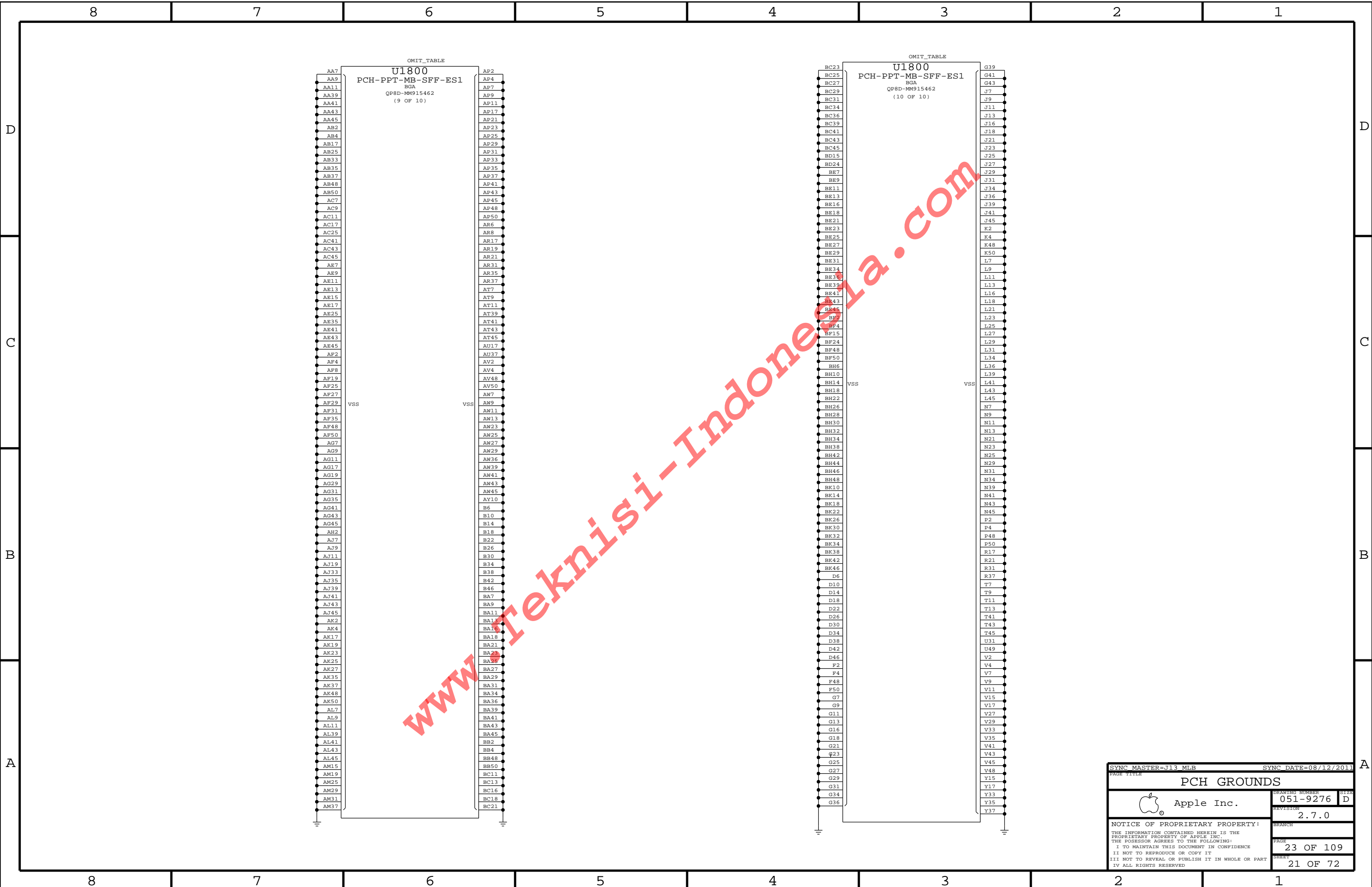
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SYNC DATE=08/12/2011

PAGE TITLE

PCH GROUNDS

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REVISION  
2.7.0

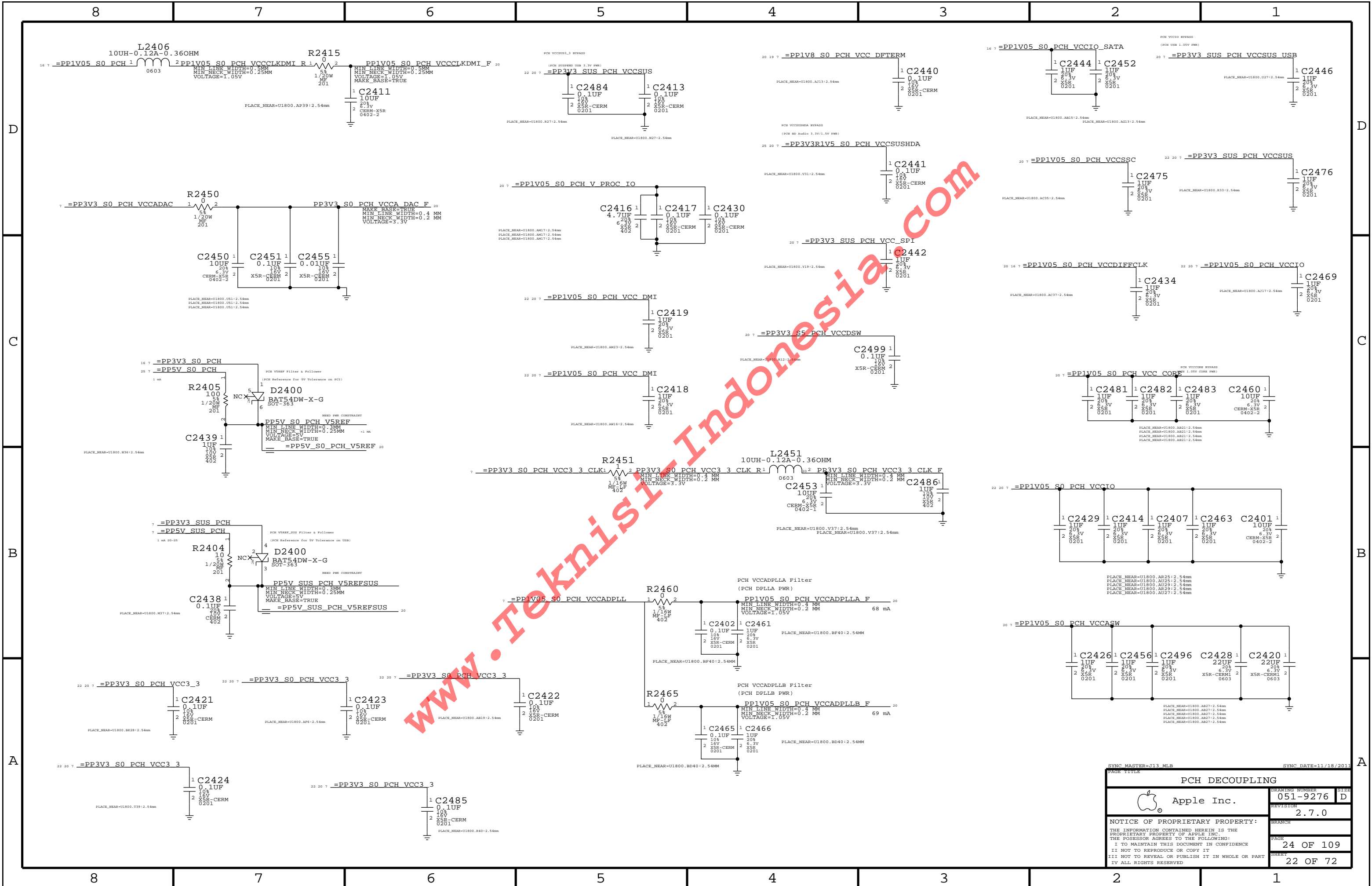
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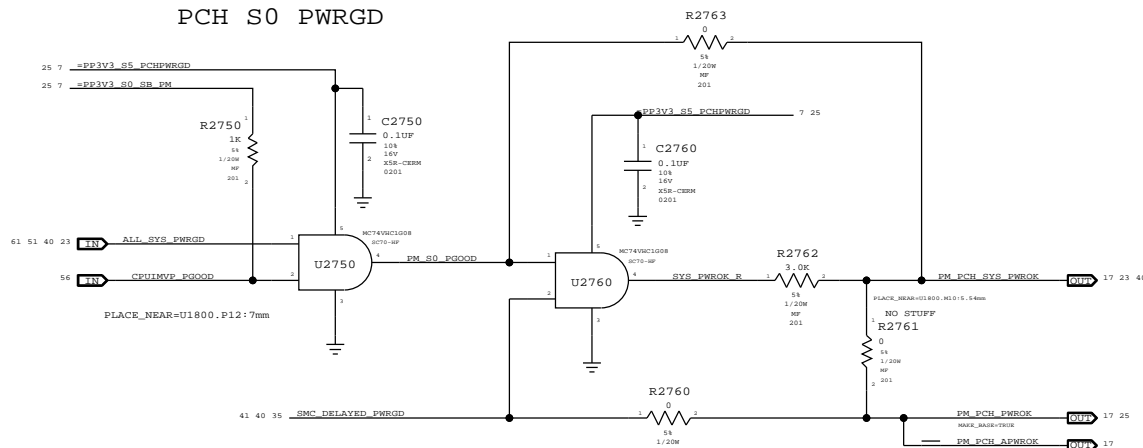
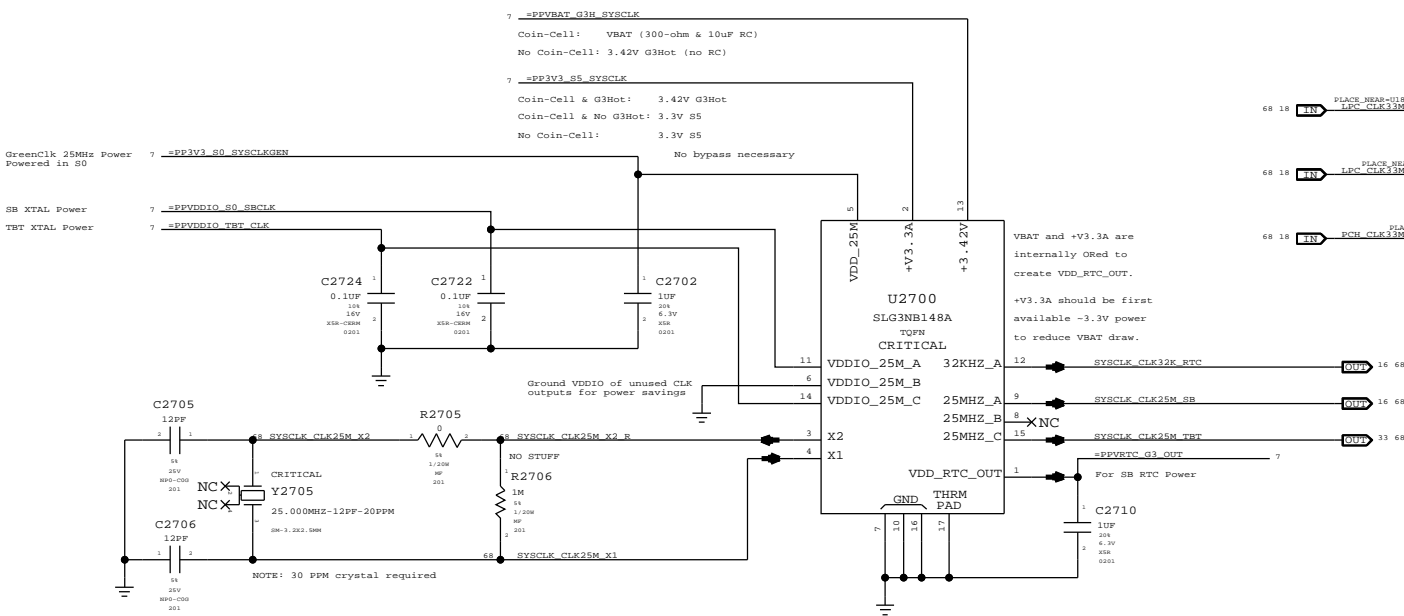




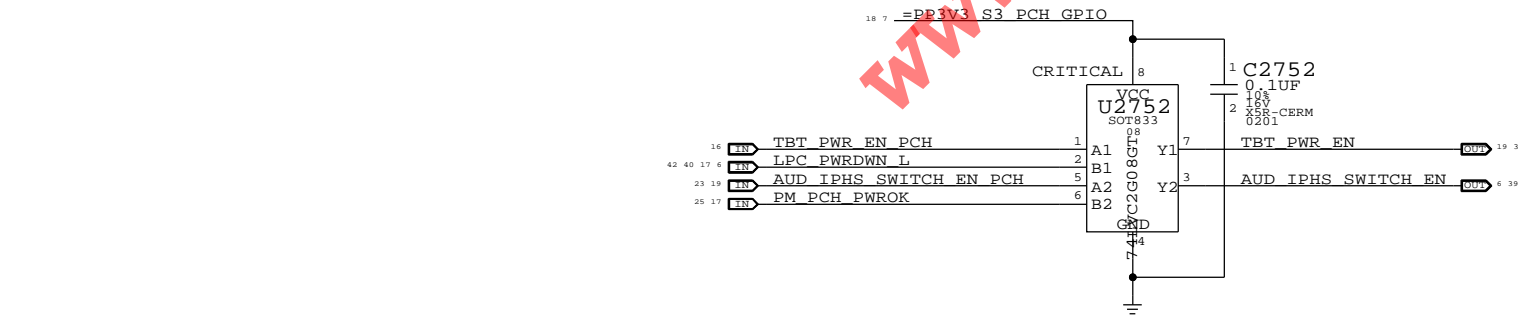




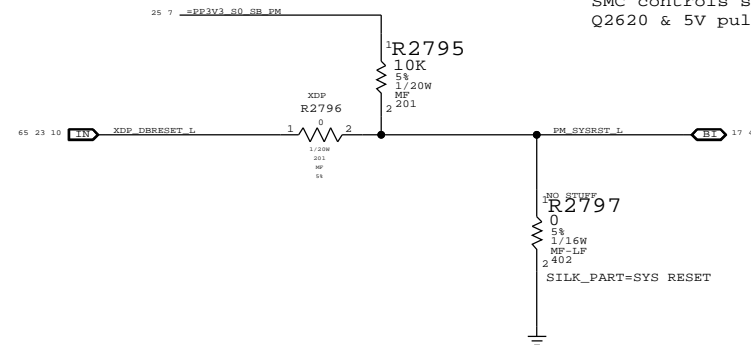
System RTC Power Source & 32kHz / 25MHz Clock Generator



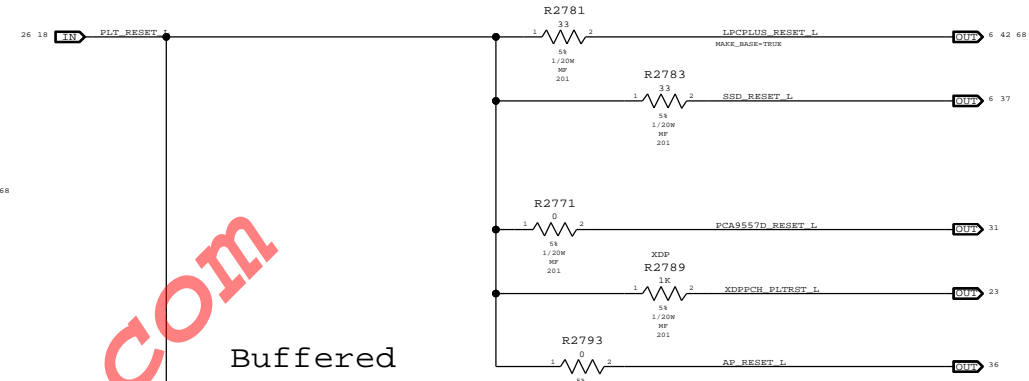
GPIO Glitch Prevention



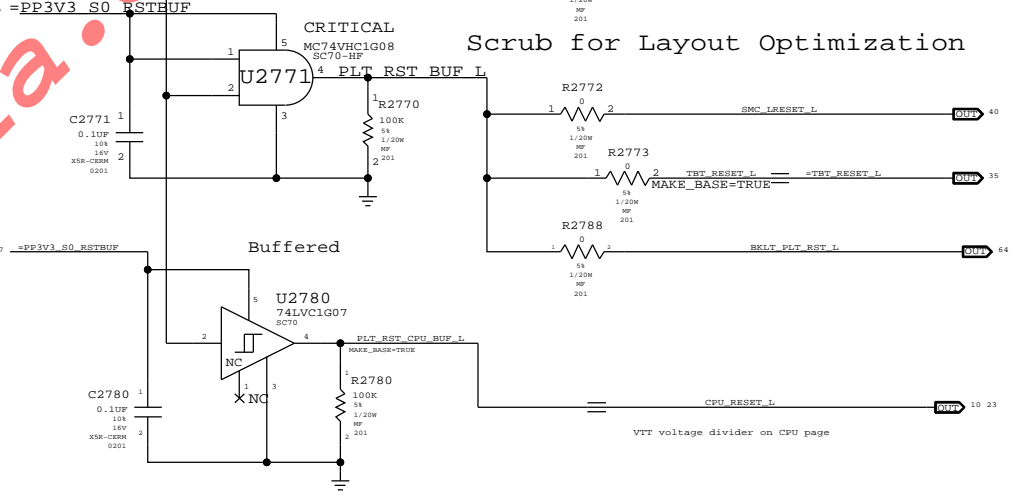
PCH Reset Button



Platform Reset Connections  
Unbuffered

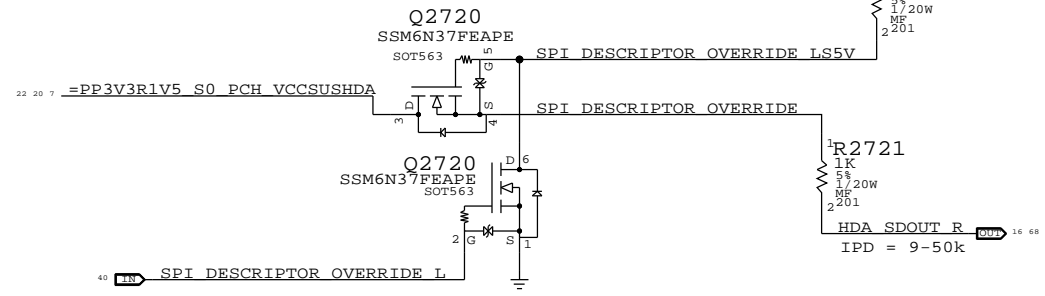


Buffered

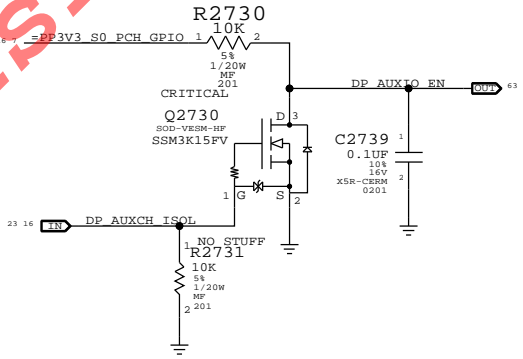


Scrub for Layout Optimization

PCH ME Disable Strap



DP\_AUXIO\_EN Inversion

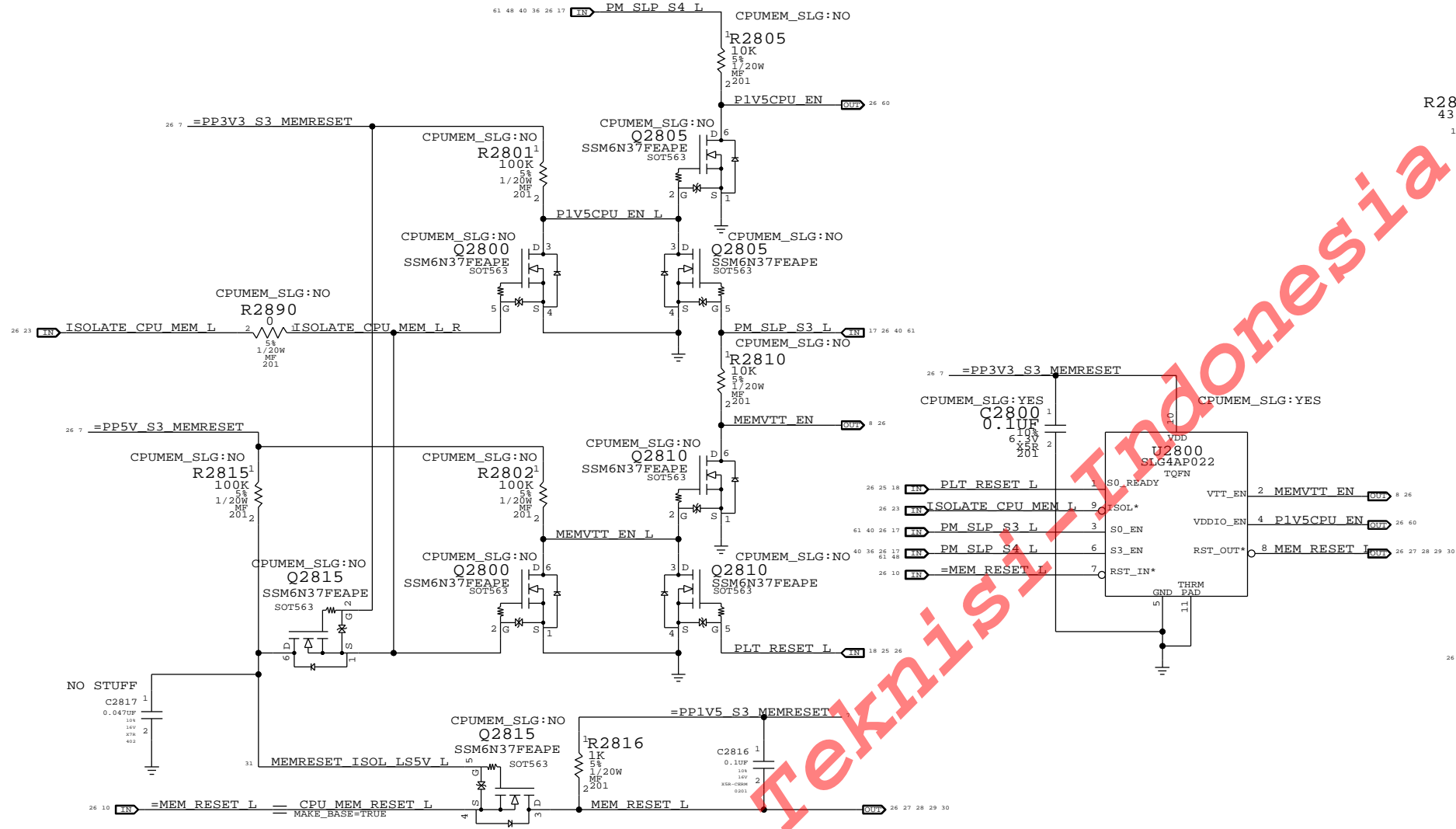


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Clock (CK505) and Chipset Support		051-9276		D			
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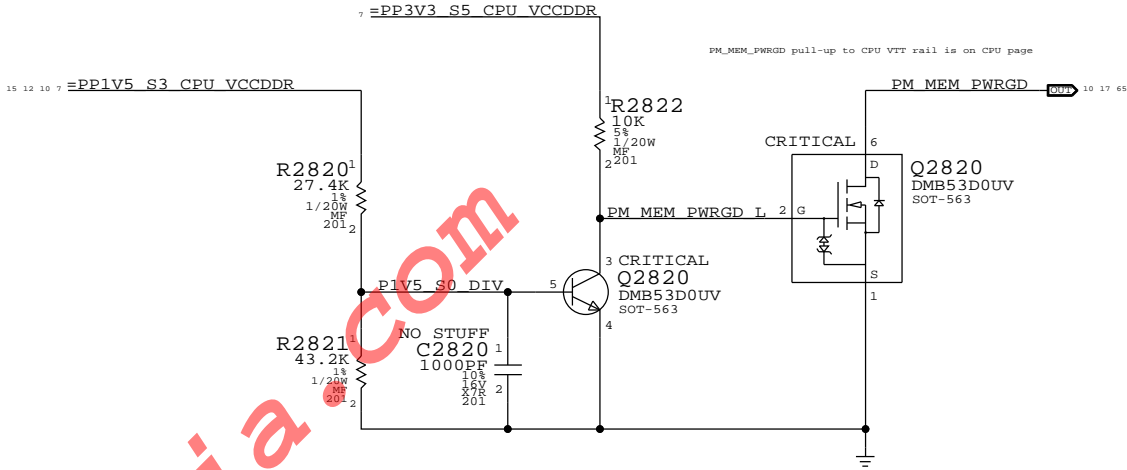
The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM\_DRAMRST# output from the S0-DIMMs when necessary.

ISOLATE\_CPU\_MEM\_L GPIO state during S3->S0 transitions determines behavior of signals.  
WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM\_RESET\_L not isolated.  
WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM\_RESET\_L isolated.

P1V5CPU\_EN = (ISOLATE\_CPU\_MEM\_L + PM\_SLP\_S3\_L) \* PM\_SLP\_S4\_L  
MEMVTT\_EN = (ISOLATE\_CPU\_MEM\_L + PLT\_RST\_L) \* PM\_SLP\_S3\_L  
MEM\_RESET\_L = !ISOLATE\_CPU\_MEM\_L + CPU\_MEM\_RESET\_L

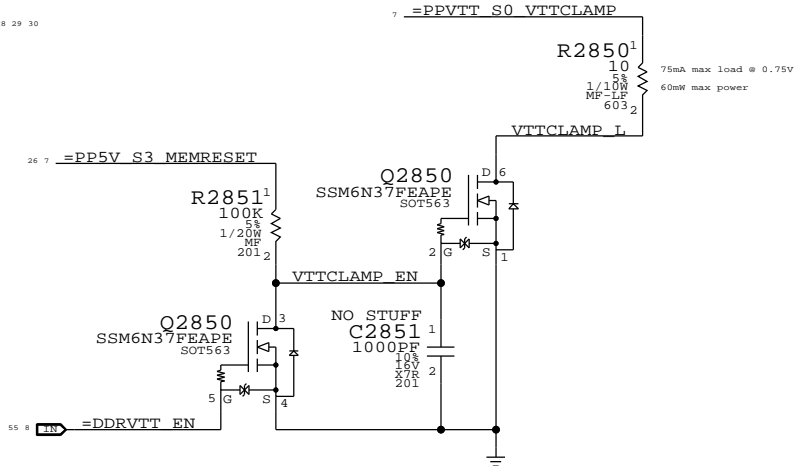


### 1V5 S0 "PGOOD" for CPU



### MEMVTT Clamp


Ensures CKE signals are held low in S3

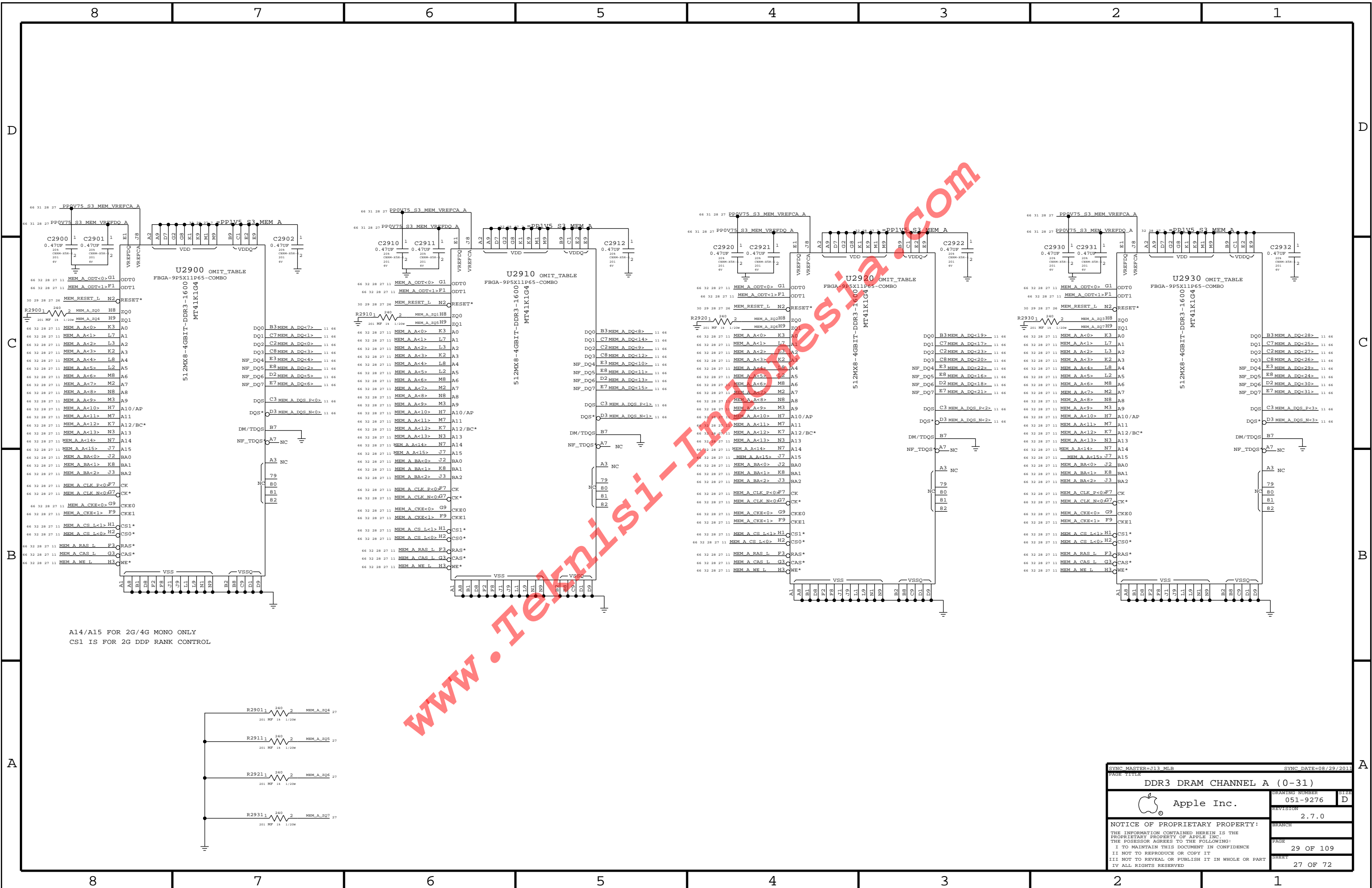


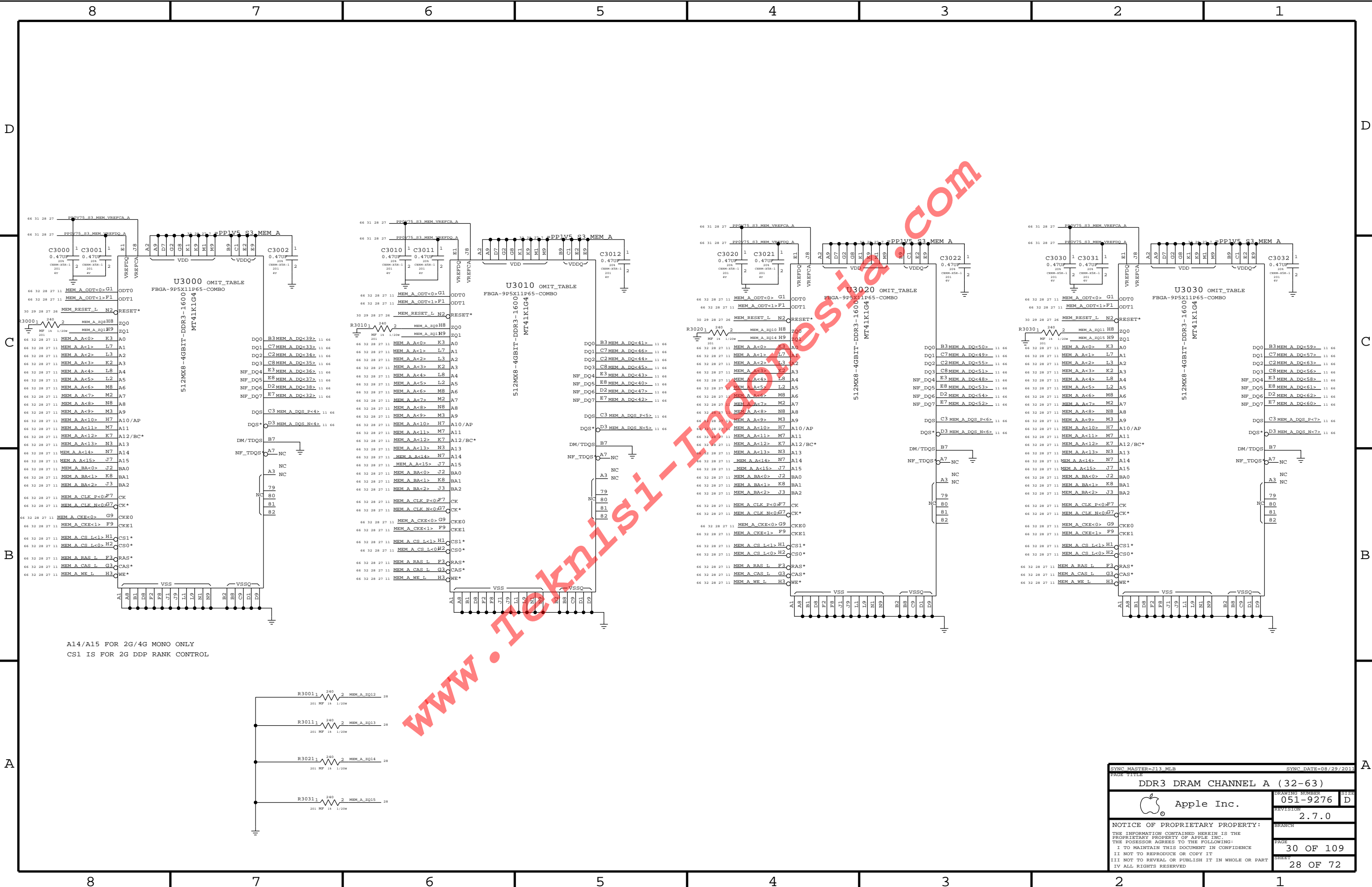
Step	ISOLATE_CPU_MEM_L	PLT_RESET_L	PM_SLP_S3_L	PM_SLP_S4_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN	P1V5CPU_EN
S0	0	1	1	1	1	CPU_MEM_RESET_L	1	1
to	1	0	1	1	1	1	1	1
2	0	0	0	1	1	0	0	1
3	0	0	0	1	X	0	0	0
S3	4	0	0	1	X	0	0	1
to	5	0	1	1	0 (*)	1	1	1
6	0	1	1	1	1	1	1	1
S0	7	1	1	1	1	CPU_MEM_RESET_L	1	1

(\*) CPU\_MEM\_RESET\_L asserts due to loss of PM\_MEM\_PWRGD, must wait for software to clear before deasserting ISOLATE\_CPU\_MEM\_L GPIO.

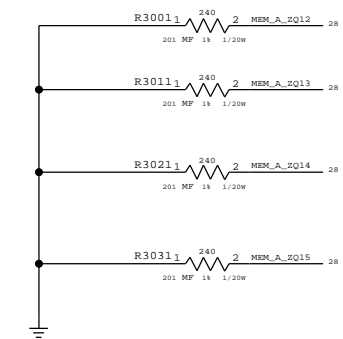
NOTE: In the event of a S3->S5 transition ISOLATE\_CPU\_MEM\_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM\_RESET\_L will not properly assert. Software must deassert ISOLATE\_CPU\_MEM\_L and then generate a valid reset cycle on CPU\_MEM\_RESET\_L.


SYNC_MASTER=513_MLP		SYNC_DATE=11/18/2013	
PAGE TITLE			
CPU Memory S3 Support			
	DRAWING NUMBER		SIZE
	051-9276	D	
Apple Inc.		REVISION	
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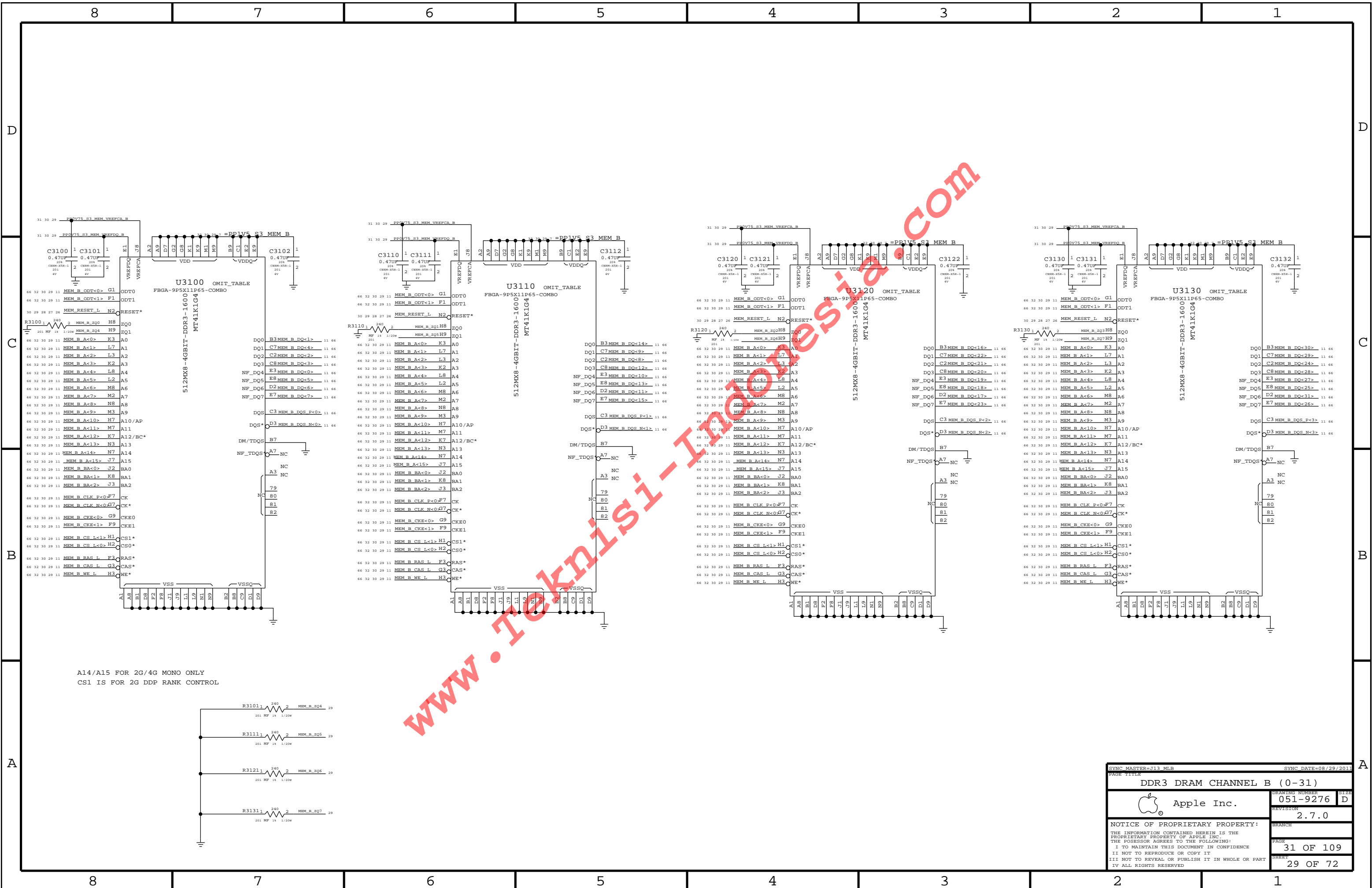


A14/A15 FOR 2G/4G MONO ONLY  
CS1 IS FOR 2G DDP RANK CONTROL

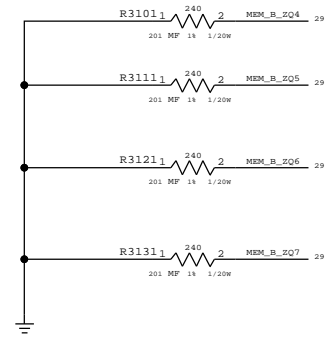



SYNC MASTER=J13 MLB		SYNC DATE=08/29/2011	
PAGE TITLE			
DDR3 DRAM CHANNEL A (32-63)			
 Apple Inc.	DRAWING NUMBER	051-9276	SIZE D
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		SHEET	28 OF 72

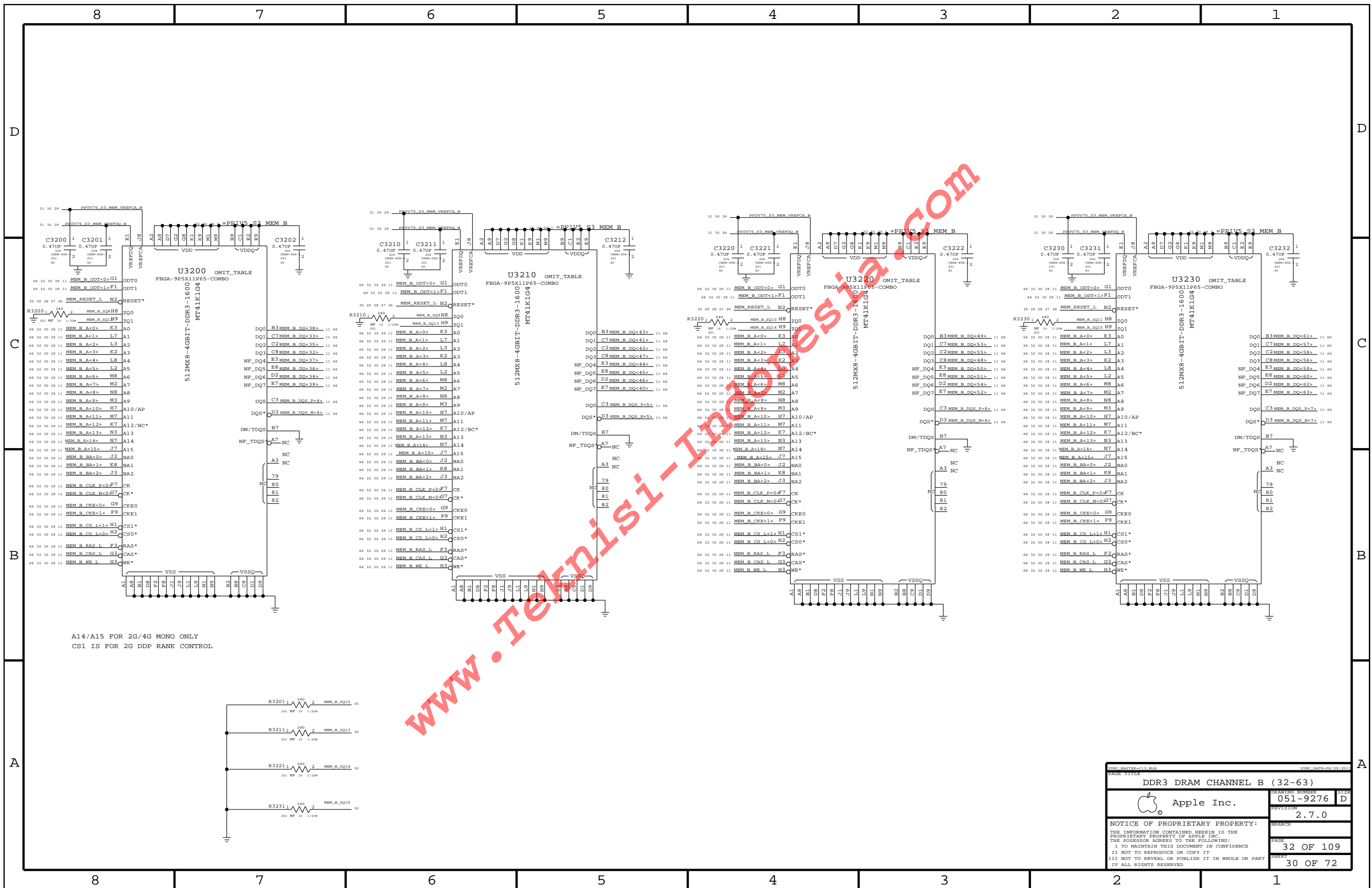




A14/A15 FOR 2G/4G MONO ONLY  
CS1 IS FOR 2G DDP RANK CONTROL



SYNC MASTER=J13 MLB		SYNC DATE=08/29/2011	
PAGE TITLE			
DDR3 DRAM CHANNEL B (0-31)			
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		SHEET	29 OF 72



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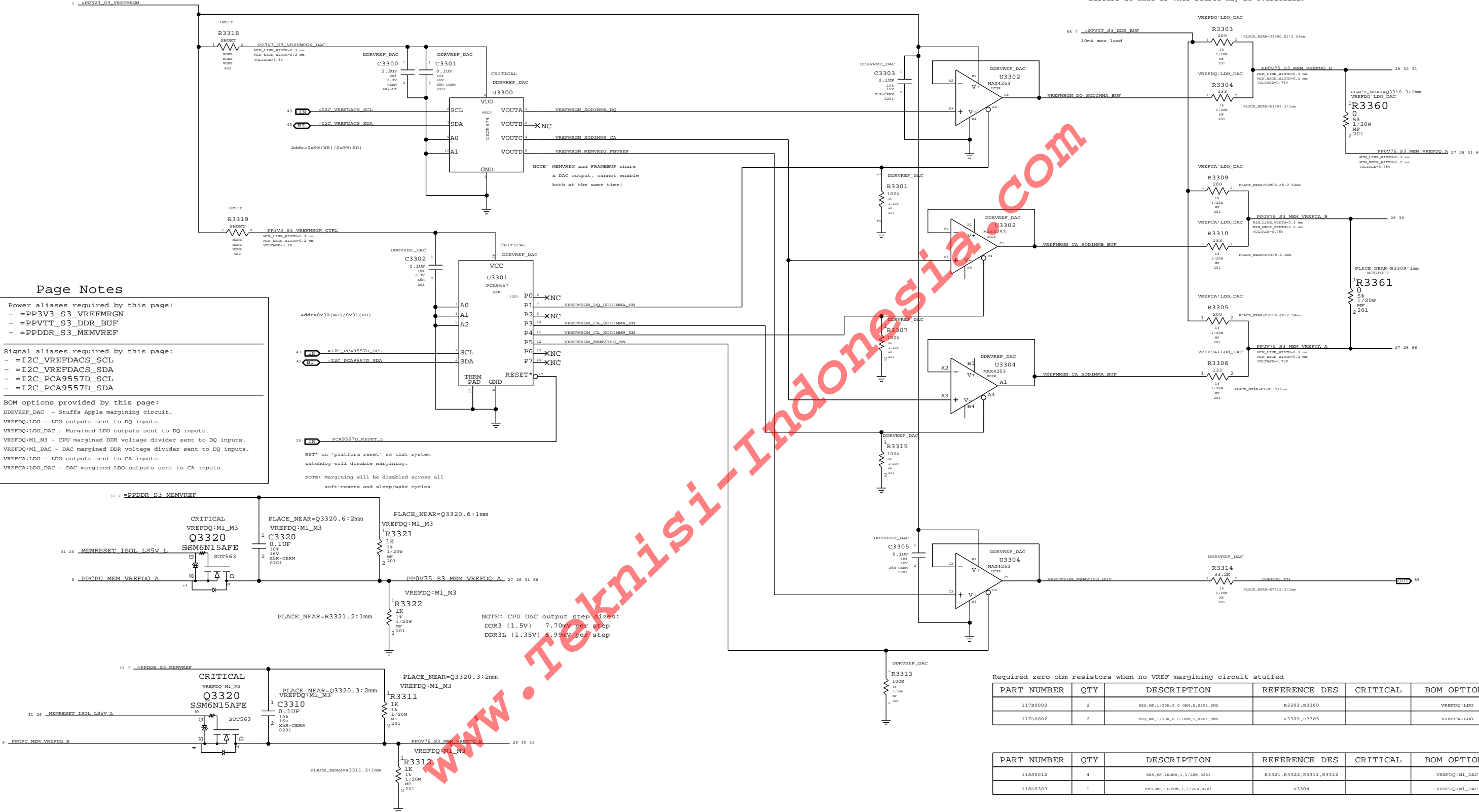
D

C

B

A

NOTE: Must not enable more than two SO-DIMM margining buffers at once or Vref source may be overloaded.



Page Notes

Power aliases required by this page:

- =PP3V3\_S3\_VREFM3
- =PPVTT\_S3\_DDR\_BUF
- =PPDDR\_S3\_MEMVREF

Signal aliases required by this page:

- =I2C\_VREFDACS\_SCL
- =I2C\_VREFDACS\_SDA
- =I2C\_PCA9557D\_SCL
- =I2C\_PCA9557D\_SDA

BOM options provided by this page:

- DDRREF\_DAC - Stuffs Apple margining circuit.
- VREFDQ:LDO - LDO outputs sent to DQ inputs.
- VREFDQ:LDO\_DAC - Margined LDO outputs sent to DQ inputs.
- VREFDQ:M1\_M3 - CPU margined DDR voltage divider sent to DQ inputs.
- VREFDQ:M1\_DAC - DAC margined DDR voltage divider sent to DQ inputs.
- VREFCA:LDO - LDO outputs sent to CA inputs.
- VREFCA:LDO\_DAC - DAC margined LDO outputs sent to CA inputs.

NOTE: Margining will be disabled across all soft-resets and sleep/wake cycles.


NOTE: CPU DAC output step sizes:  
DDR3 (1.5V) 7.70mV per step  
DDR3L (1.35V) 6.99mV per step

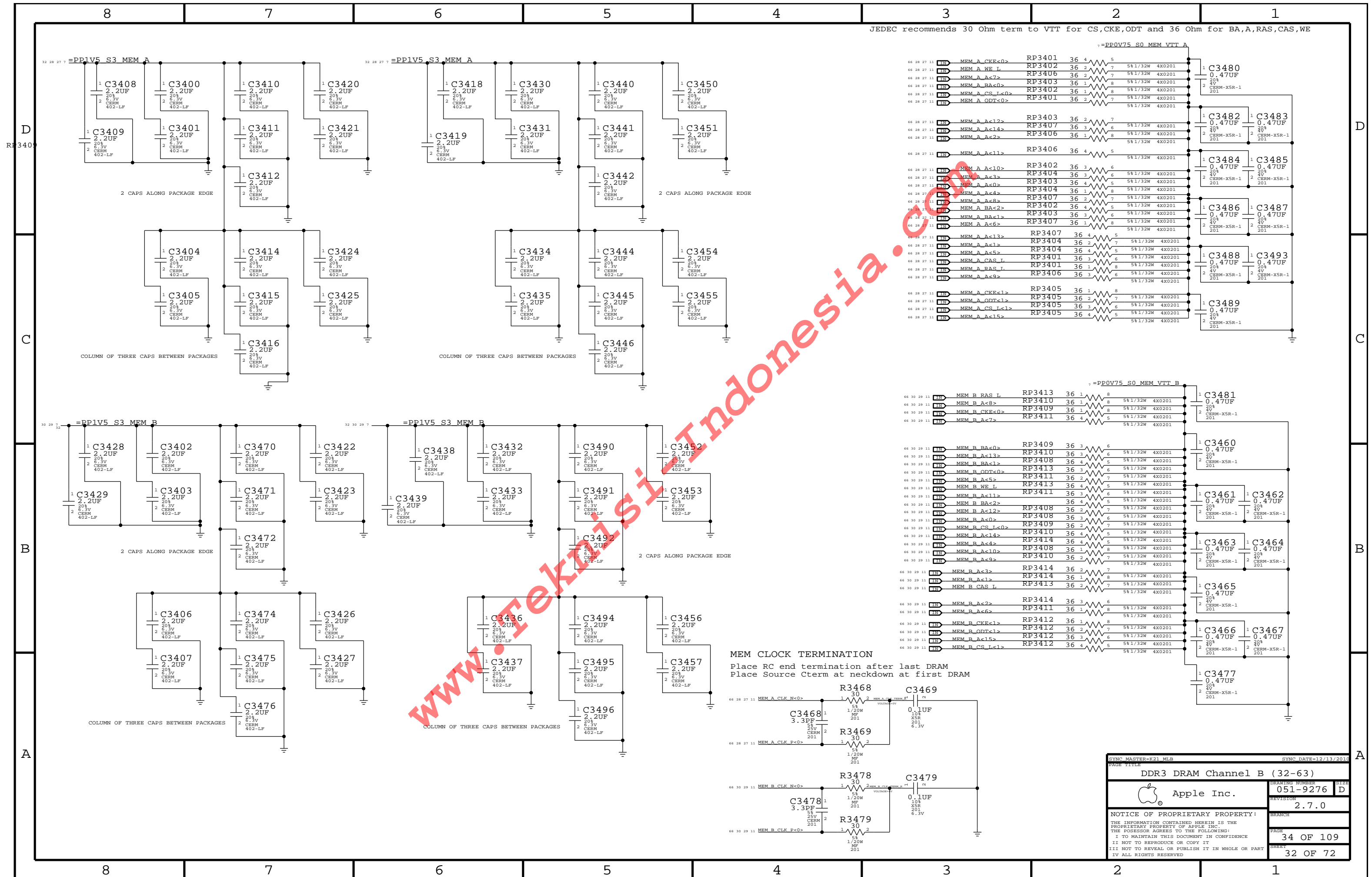
Required zero ohm resistors when no Vref margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
11780002	2	RES,MP,1/20W,0.0 OHM,5,0201,SMD	R3303,R3360		VREFDQ:LDO
11780002	2	RES,MP,1/20W,0.0 OHM,5,0201,SMD	R3309,R3305		VREFCA:LDO

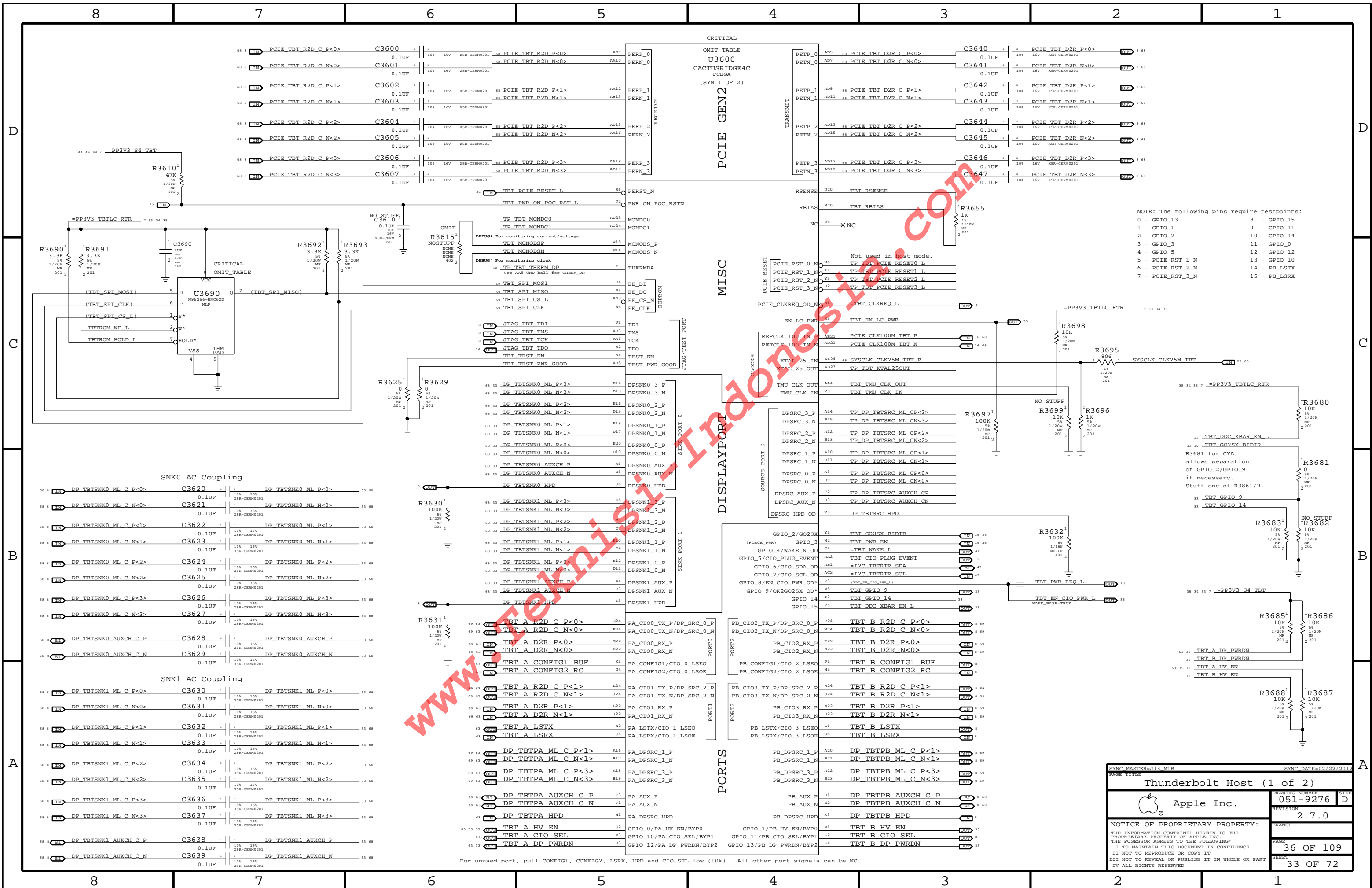
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
11880012	4	RES,MP,1KOHM,1,1/20W,0201	R3321,R3322,R3311,R3312		VREFDQ:M1_DAC
11880003	1	RES,MP,3320OHM,1,1/20W,0201	R3304		VREFDQ:M1_DAC

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	GPU Frame Buffer (1.8V, 70% Vref)
DAC Channel:	A	B	C	C	D	D
PCA9557D Pin:	1	2	3	4	5	6
Nominal value		0.75V (DAC: 0x3A)			1.5V (DAC: 0x3A)	1.267V (DAC: 0x8B)
Margined target:		0.300V - 1.200V (+/- 450mV)			1.000V - 2.000V (+/- 500mV)	1.056V - 1.442V (+/- 180mV)
DAC range:		0.000V - 1.501V (0x00 - 0x74)			0.000V - 3.000V (0x00 - 0xFF)	0.000V - 3.300V (0x00 - 0xFF)
Vref current:		+3.4mA - -3.4mA (- = sourced)			+61uA - -61uA (- = sourced)	+6.0mA - -5.0mA (- = sourced)
DAC step size:		7.69mV / step @ output			8.59mV / step @ output	1.51mV / step @ output

SYMC PARTSHEET:113 MEM		SYMC DATE:11/18/2011	
PAGE TITLE			
FSB/DDR3/FRAMEBUF Vref Margining			
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		REVISION	2.7.0
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SYNC DATE=03/22/2012

Thunderbolt Host (1 of 2)

Apple Inc.

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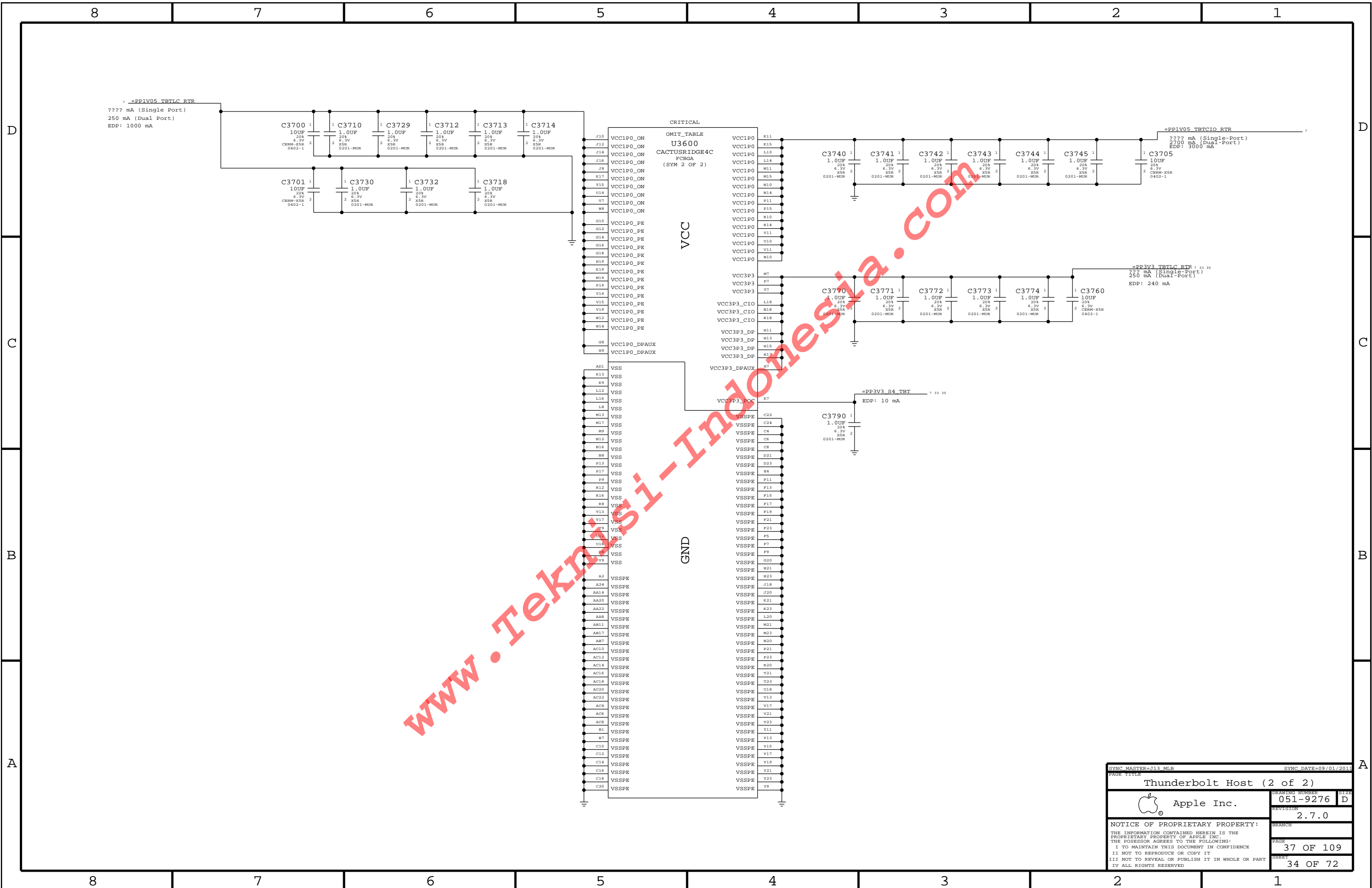
DRAWING NUMBER  
051-9276

REVISION  
2.7.0

PAGE  
36 OF 109

SHEET  
33 OF 72





Power aliases required by this page:

- =PPVIN\_SW\_TBTBST (8-13V Boost Input)
- =PP18V\_TBT\_REG (18V Boost Output)
- =PP3V3\_TBT\_P3V3TBTFT (3.3V FET Input)
- =PP3V3\_TBT\_FET (3.3V FET Output)
- =PP3V3\_S0\_TBTPWRCTL
- =PP1V05\_TBT\_P1V05TBTFT (1.05V FET Input)
- =PP1V05\_TBT\_FET (1.05V FET Output)

---

Signal aliases required by this page:

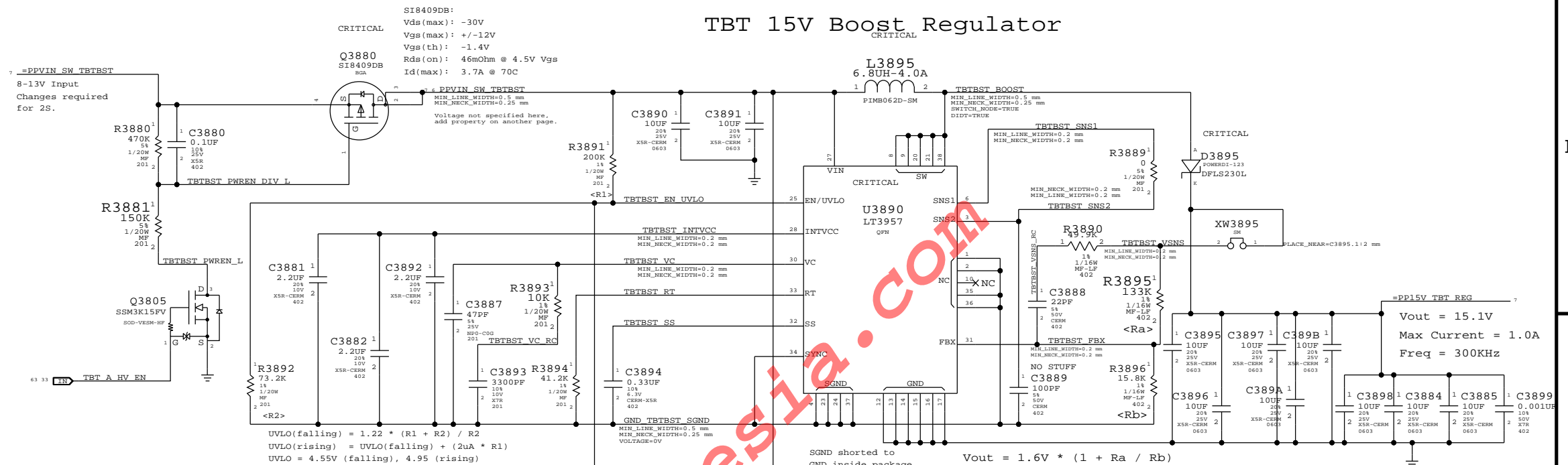
- =TBT\_CLKREQ\_L
- =TBT\_RESET\_L

---

BOM options provided by this page:

TBTBST:Y - Stuffs 18V boost circuitry.

BOM options provided by this page:  
TBTBST:Y - Stuffs 18V boost circuitry

[illegible][illegible]

33 7 =PP3V3 S4 TBT

CRITICAL

VDD

Pull-up: R3610

2 SENSE U3830 RESET\* TBT\_PWR\_ON\_POC\_RST\_L 33

TPS3808

3 CT TBTPOCRST\_MR\_L

QFN

(12V) MR\*

GND

THTM PAD

TPS3808G25

Vt = 2.33V +/- 2%

Delay = 27.3ms

1 C3831 0.0047UF 1% 25V C3830 402

C3830 1 0.1UF 10% 16V XSR-C3830 9201 2

Q3825 SSM6N37FEAPE SOT563

R3830 1 100K 1% 1/20W XSR-R3830 2501

TBT SW RESET\_L 19

C3825 1 3300PF 10% 16V XSR-C3825 201 2

C3825 value may need tuning

=PP3V3 S0 PCH GPIO 7 16 17 18 19 20


[illegible]

Part	TPS22920
Type	Load Switch
R(on)	8 mOhm Typ
@ 1.05V	11.5 mOhm Max

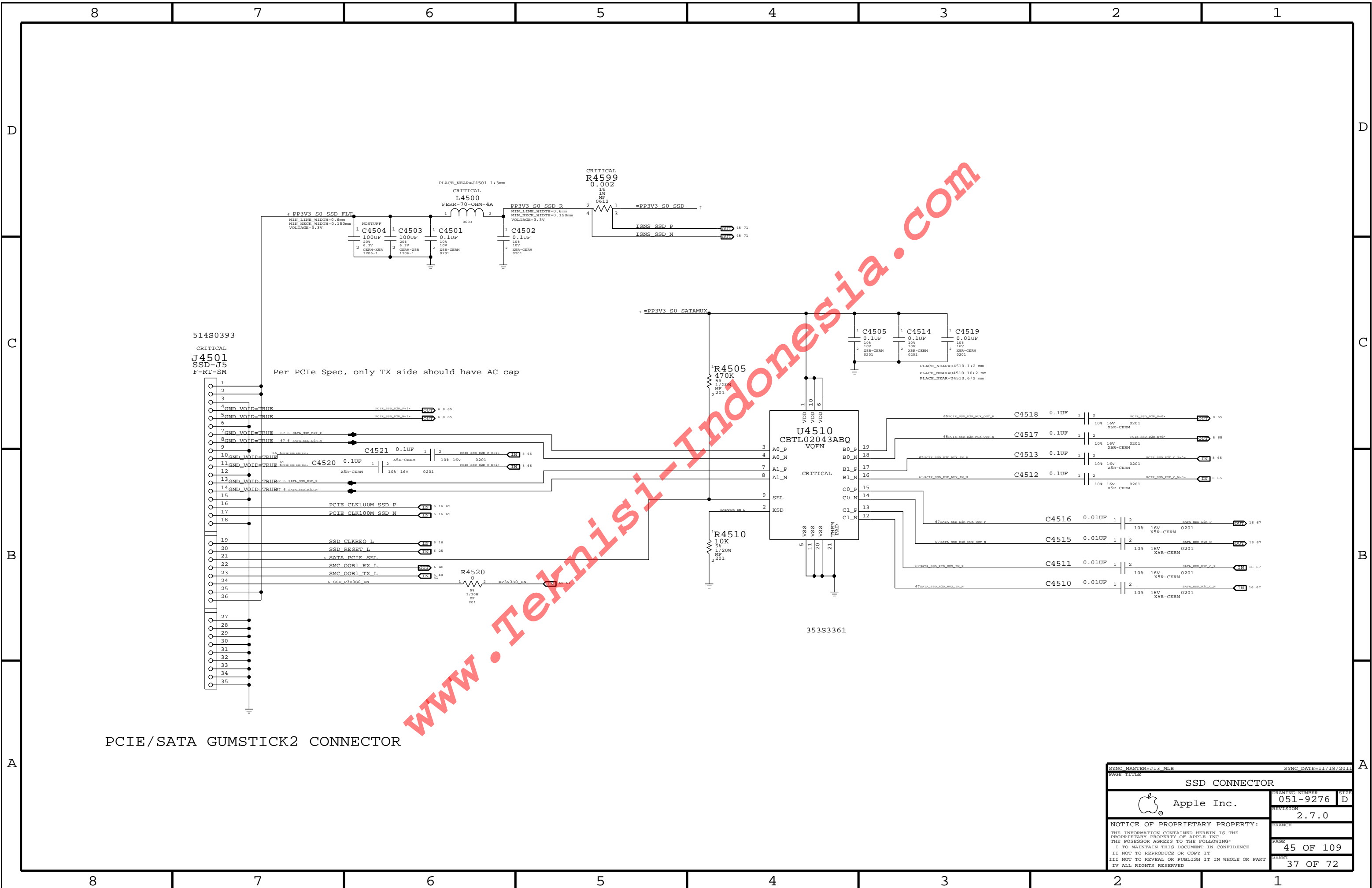
Part	TPS22924C
Type	Load Switch
R(on)	20.3 mOhm Typ
@ 1.0V	28.6 mOhm Max

C3816 must be 10%


RC guarantees minimum 5ms to reach 0.5V

SYNC MASTER=J13 M1B		SYNC DATE=11/18/2011	
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TBT Power Support			
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		PAGE	38 OF 109
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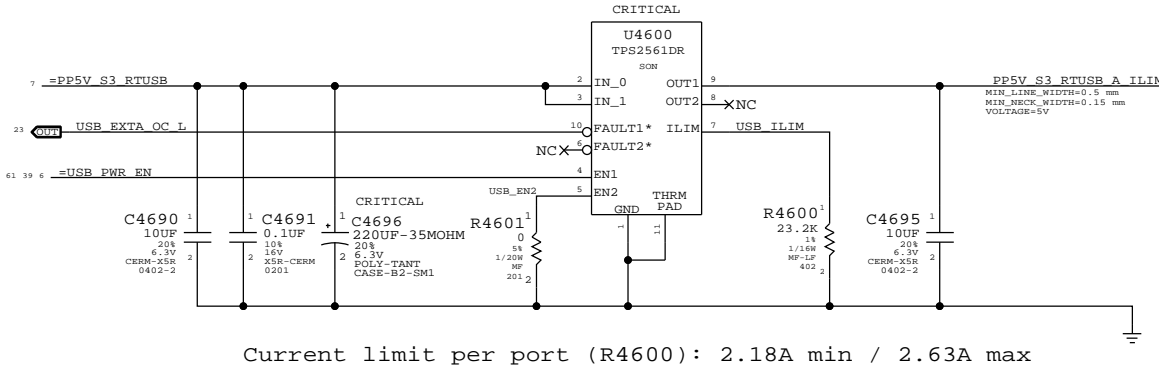


PCIE/SATA GUMSTICK2 CONNECTOR

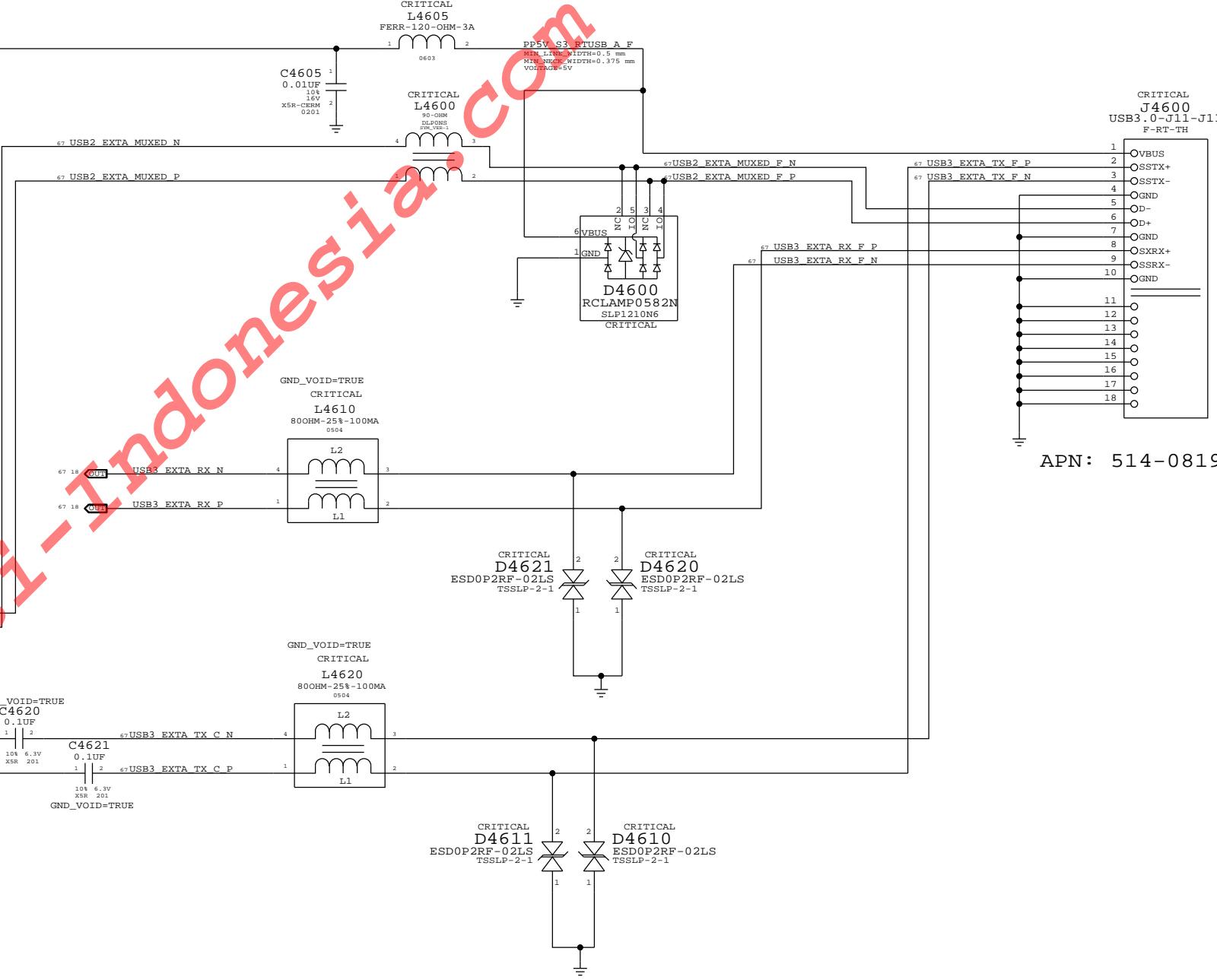
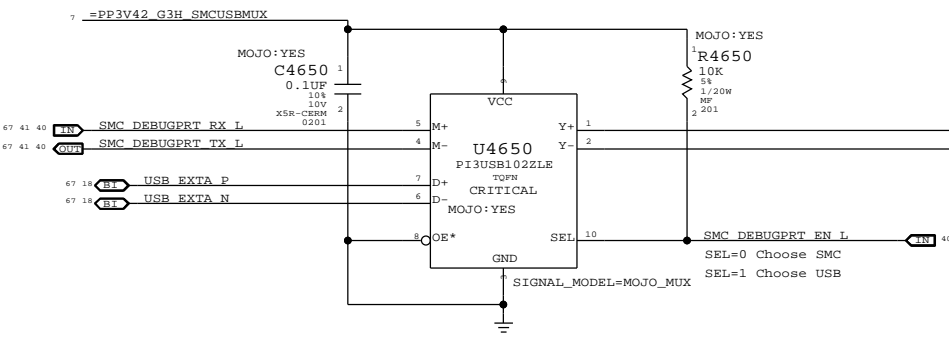
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SSD CONNECTOR			
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Right USB Port A


USB Port Power Switch



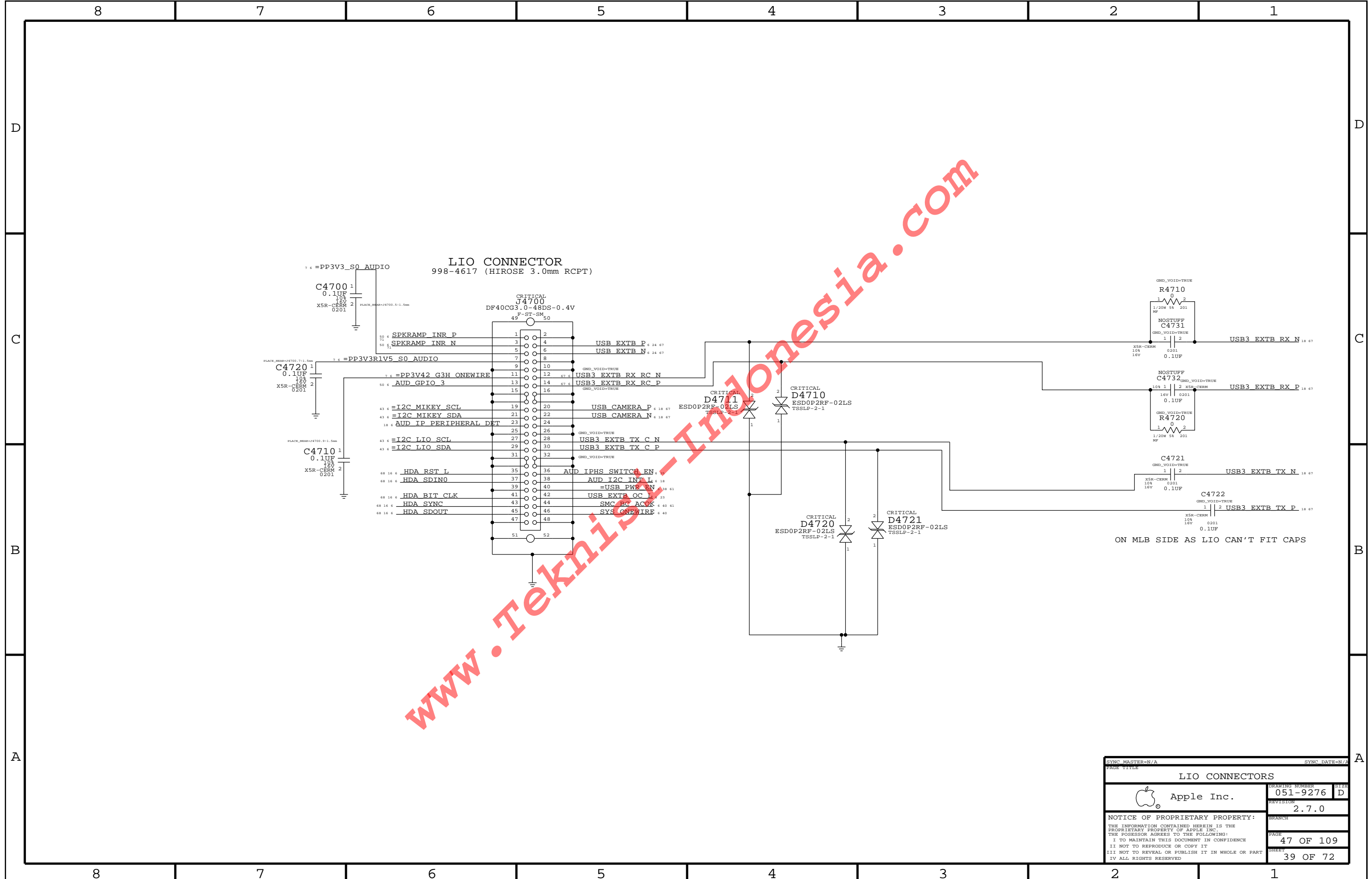
Mojo SMC Debug Mux




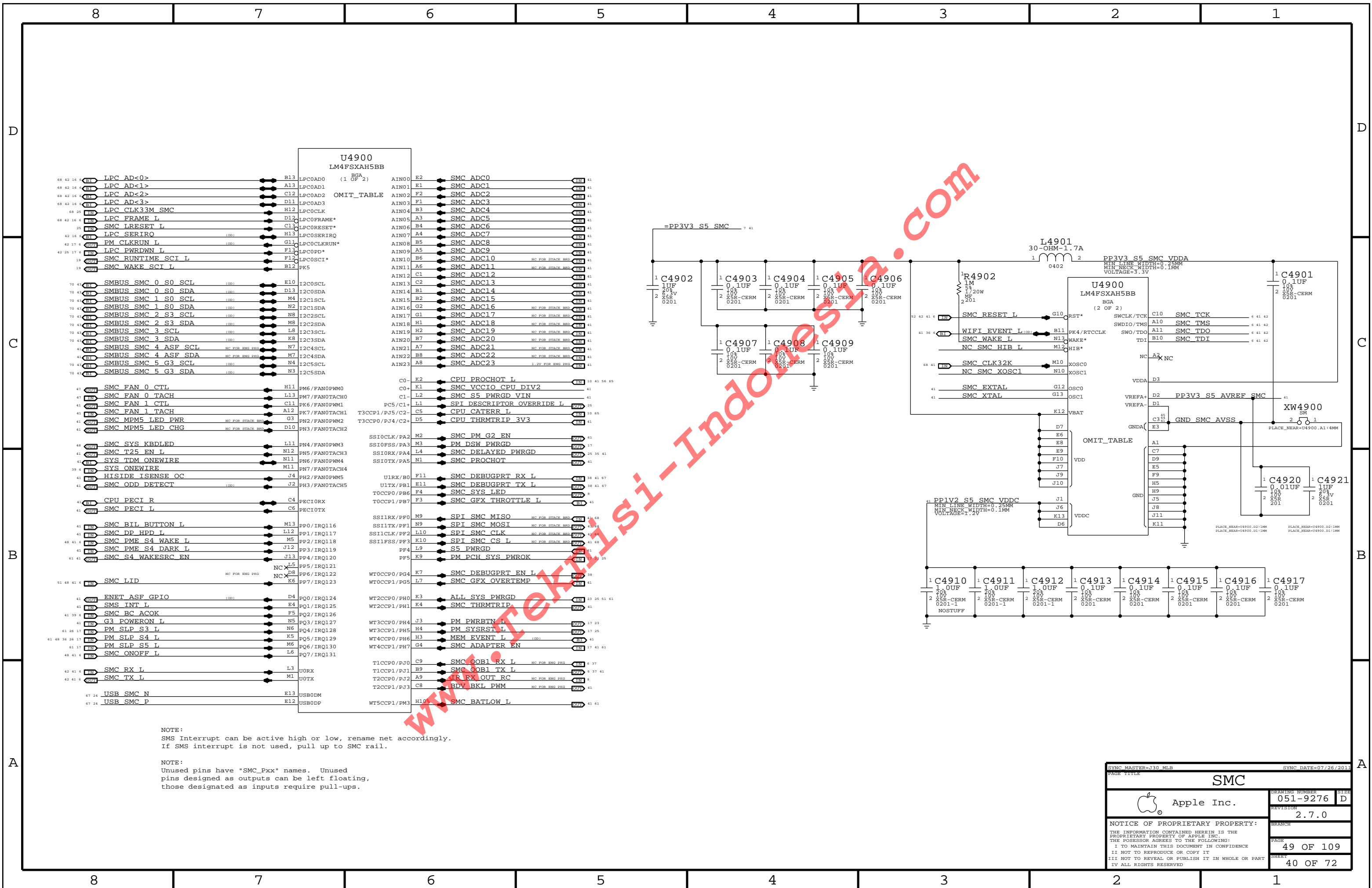
APN: 514-0819

SYNC MASTER=J13 MLB		SYNC DATE=10/06/2013	
PAGE TITLE			
External A USB3 Connector			
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8	7	6	5	4	3	2	1
---	---	---	---	---	---	---	---



## C



## A

8	7	6	5	4	3	2	1
---	---	---	---	---	---	---	---

	5	
--	---	--

	5	
--	---	--



SSM3K15AMFVAPE



A horizontal number line with arrows at both ends. There are 11 vertical tick marks labeled 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, and 10 from left to right. Below the line, the number '2' is centered under the tick mark for 2, and the number '1' is centered under the tick mark for 8.

LPCPLUS  
 CRITICAL  
 J5100  
 DF40C-30DP-0.4V  
 M-ST-SM

7 6 =PP3V3 S5 LPCPLUS  
 7 6 =PP5V S0 LPCPLUS

68 25 6 **ST** LPC CLK33M LPCPLUS  
 68 40 16 **ST** LPC AD<0>  
 68 40 16 **ST** LPC AD<2>  
 68 40 16 **ST** LPC AD<1>  
 68 40 16 **ST** LPC AD<3>  
 42 6 **ST** SPI ALT MOSI  
 19 6 **ST** LPCPLUS GPIO  
 68 25 6 **ST** LPCPLUS RESET L  
 41 40 6 **ST** SMC TDO  
 6 41 40 6 **ST** TP SMC TRST L  
 6 41 40 6 **ST** TP SMC MD1  
 41 40 6 **ST** SMC TX L

1 2  
 3 4  
 5 6  
 7 8  
 9 10  
 11 12  
 13 14  
 15 16  
 17 18  
 19 20  
 21 22  
 23 24  
 25 26  
 27 28  
 29 30  
 33 34

SPI ALT MISO  
 LPC FRAME L  
 SPIROM USE MLB  
 PM CLKRUN L  
 SPI ALT CLK  
 SPI ALT CS L  
 LPC SERIRQ  
 LPC PWRDWN L  
 SMC TDI  
 SMC TCK  
 SMC RESET L  
 SMC ROMBOOT  
 SMC RX L  
 SMC TMS

6 42  
 6 16 40 6  
 6 19 49  
 6 17 40  
 6 42  
 6 42  
 6 16 40  
 6 17 28 40  
 40 41  
 40 41  
 6 41  
 6 40 41  
 6 41  
 6 40 41

998-4235

**Channel R:**  
 R5110: 24.9Ω, 1/20W MF 201, PLACE\_NEAR=U1800.AB8:5mm  
 R5111: 15Ω, 1/20W MF 201, PLACE\_NEAR=U1800.AD12:5mm  
 R5112: 15Ω, 1/20W MF 201, PLACE\_NEAR=U1800.W8:5mm

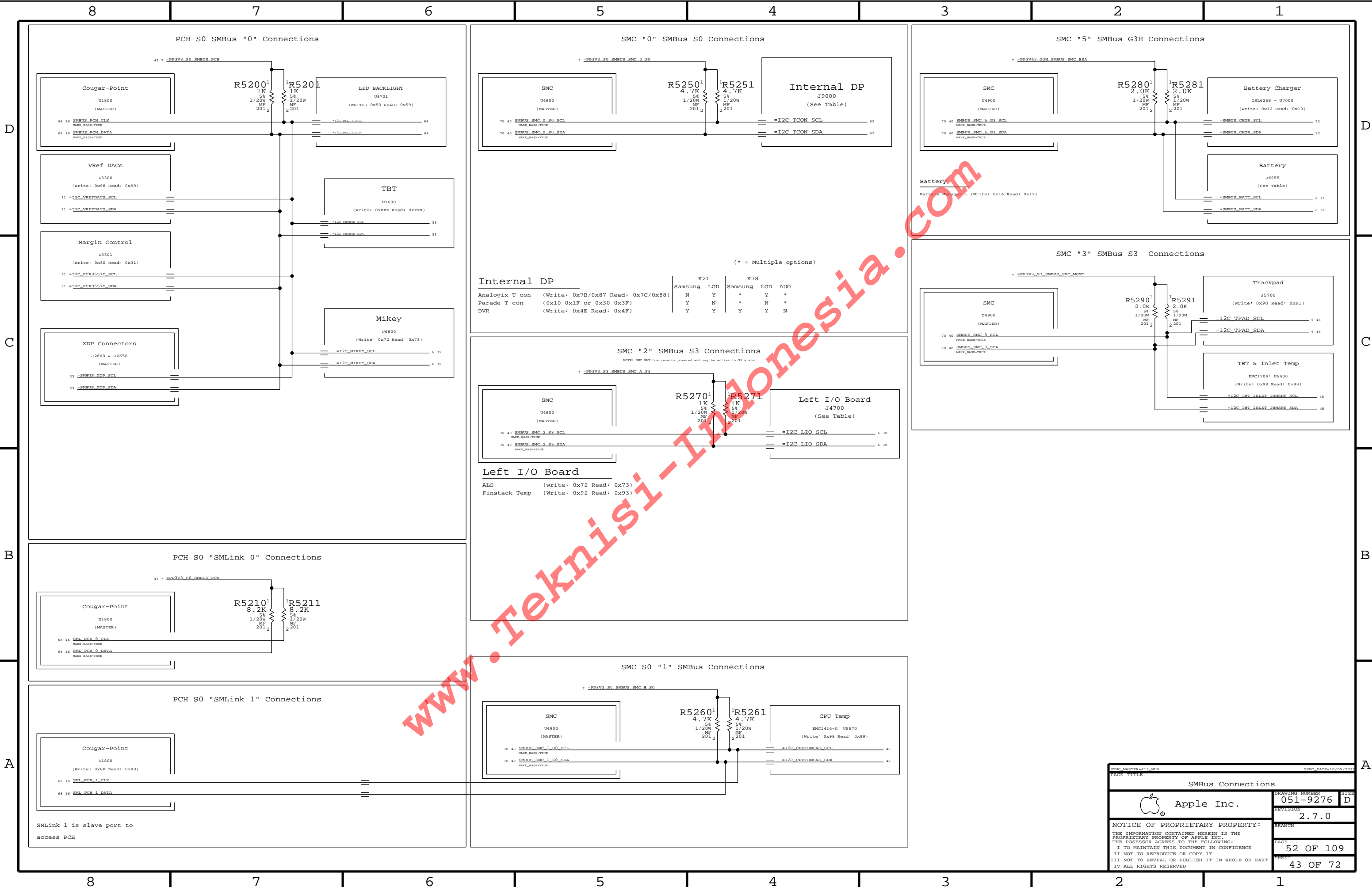
**Channel L:**  
 R5120: 43Ω, 1/20W MF 201, PLACE\_NEAR=R5125.2:5mm  
 R5121: 43Ω, 1/20W MF 201, PLACE\_NEAR=R5126.2:5mm  
 R5122: 43Ω, 1/20W MF 201, PLACE\_NEAR=R5127.2:5mm  
 R5123: 24.9Ω, 1/20W MF 201, PLACE\_NEAR=U6100.2:5mm

**Channel CLK:**  
 R5113: 15Ω, 1/20W MF 201, PLACE\_NEAR=U1800.AB8:5mm  
 R5114: 15Ω, 1/20W MF 201, PLACE\_NEAR=U1800.AD12:5mm  
 R5115: 15Ω, 1/20W MF 201, PLACE\_NEAR=U1800.W8:5mm

**Channel CS:**  
 R5116: 15Ω, 1/20W MF 201, PLACE\_NEAR=U1800.AB8:5mm  
 R5117: 15Ω, 1/20W MF 201, PLACE\_NEAR=U1800.AD12:5mm  
 R5118: 15Ω, 1/20W MF 201, PLACE\_NEAR=U1800.W8:5mm

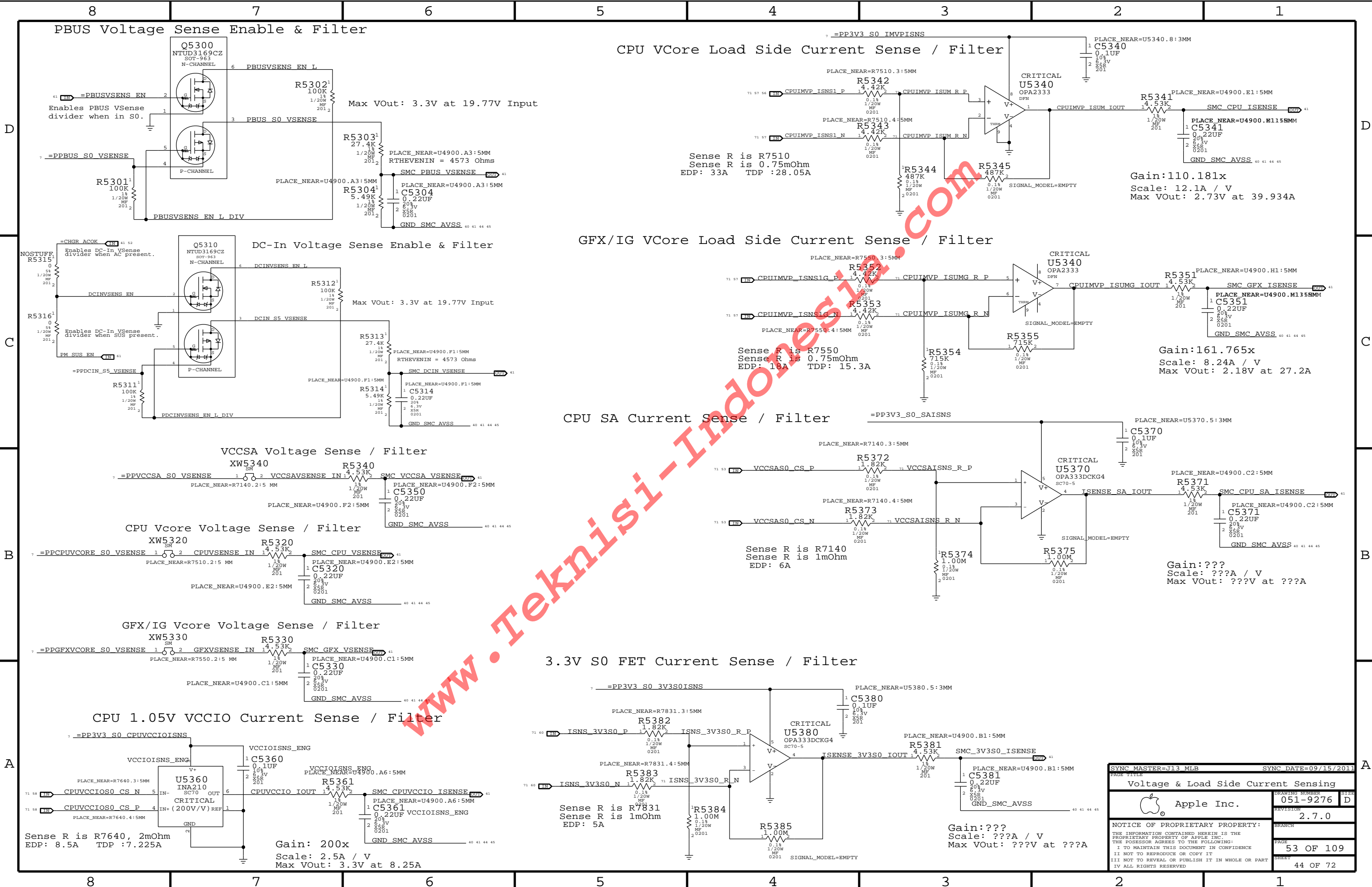
**Channel CS L:**  
 R5119: 15Ω, 1/20W MF 201, PLACE\_NEAR=U1800.AB8:5mm  
 R5120: 15Ω, 1/20W MF 201, PLACE\_NEAR=U1800.AD12:5mm  
 R5121: 15Ω, 1/20W MF 201, PLACE\_NEAR=U1800.W8:5mm


**Channel CS L:**  
 R5122: 15Ω, 1/20W MF 201, PLACE\_NEAR=U1800.AB8:5mm  
 R5123: 15Ω, 1/20W MF 201, PLACE\_NEAR=U1800.AD12:5mm  
 R5124: 15Ω, 1/20W MF 201, PLACE\_NEAR=U1800.W8:5mm

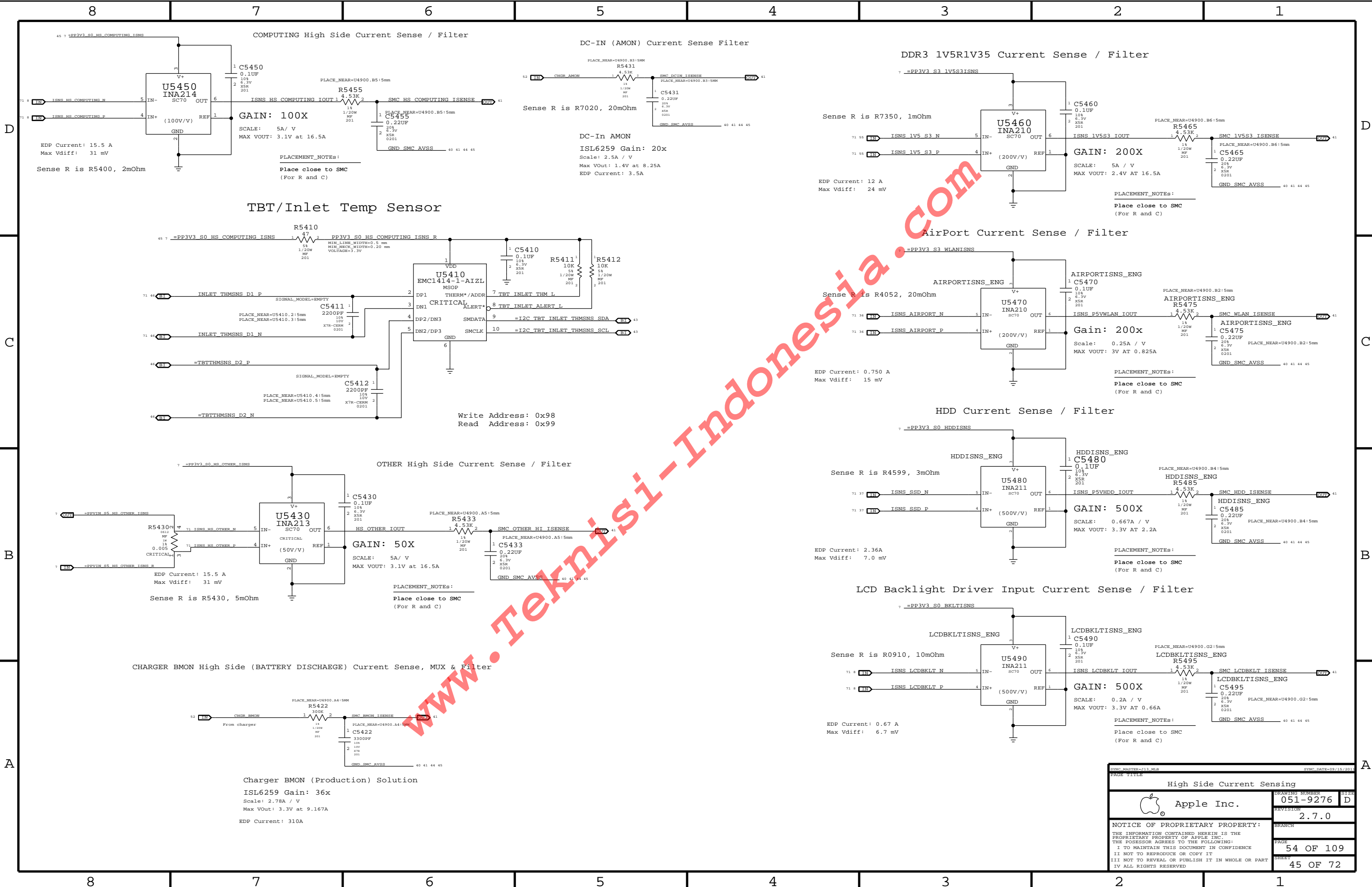



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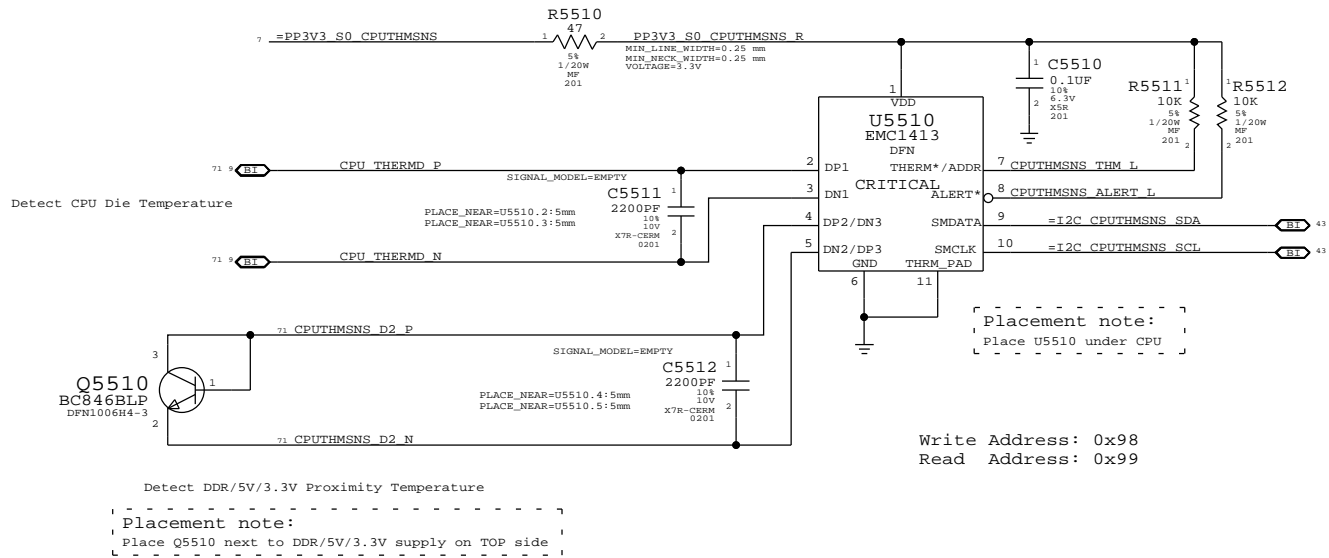


SYNC MASTER=J13 MLB		SYNC DATE=09/15/2011	
PAGE TITLE		Voltage & Load Side Current Sensing	
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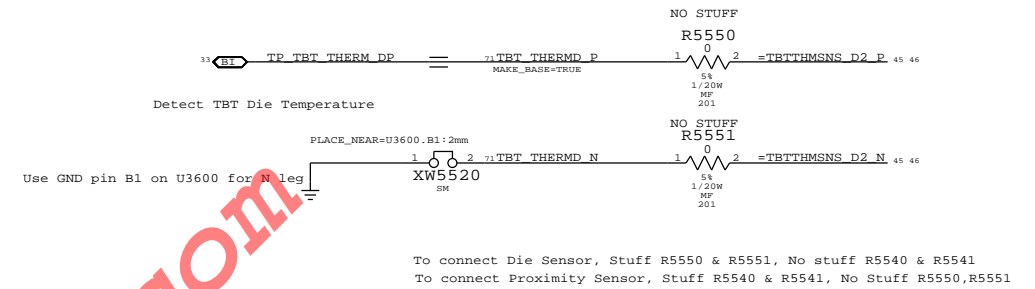


SYMC MASTER=113 MCB		SYMC DATE=09/15/2011	
PAGE TITLE			
High Side Current Sensing			
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CPU Proximity Sensor



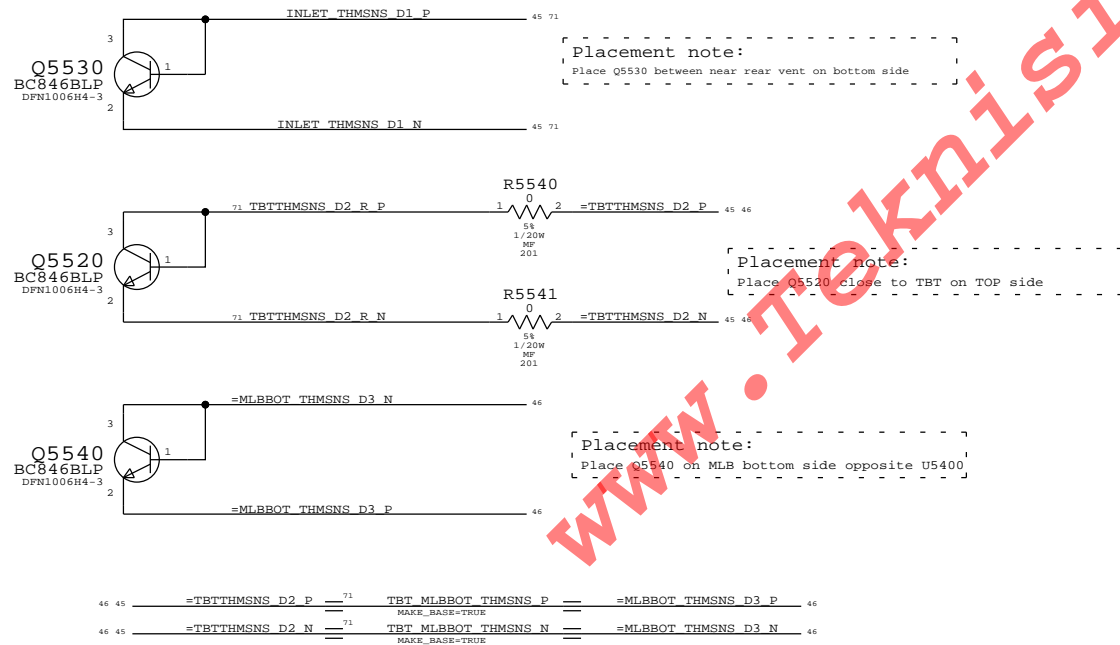
TBT Die




PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES,MP,1/20W,100K OHM,5,0201,0MD	C5361		VCCIOISNS_PROD
117S0008	1	RES,MP,1/20W,100K OHM,5,0201,0MD	C5475		AIRPORTISNS_PROD
117S0008	1	RES,MP,1/20W,100K OHM,5,0201,0MD	C5485		HDDISNS_PROD
117S0008	1	RES,MP,1/20W,100K OHM,5,0201,0MD	C5495		LCDBKLTISNS_PROD

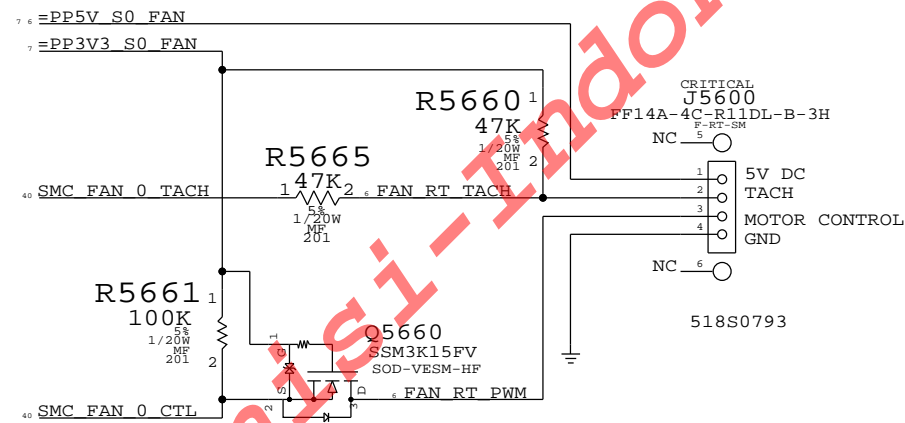
Replacing caps with 100K PD on ISENSE SMC inputs


TBT,MLB Bottom & Inlet Proximity Sensors



SYNC MASTER=J13 MLB		SYNC DATE=08/30/2013	
PAGE TITLE			
Thermal Sensors			
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FAN CONNECTOR



SYNC MASTER=K21 MLB		SYNC DATE=12/13/2010	
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Fan			
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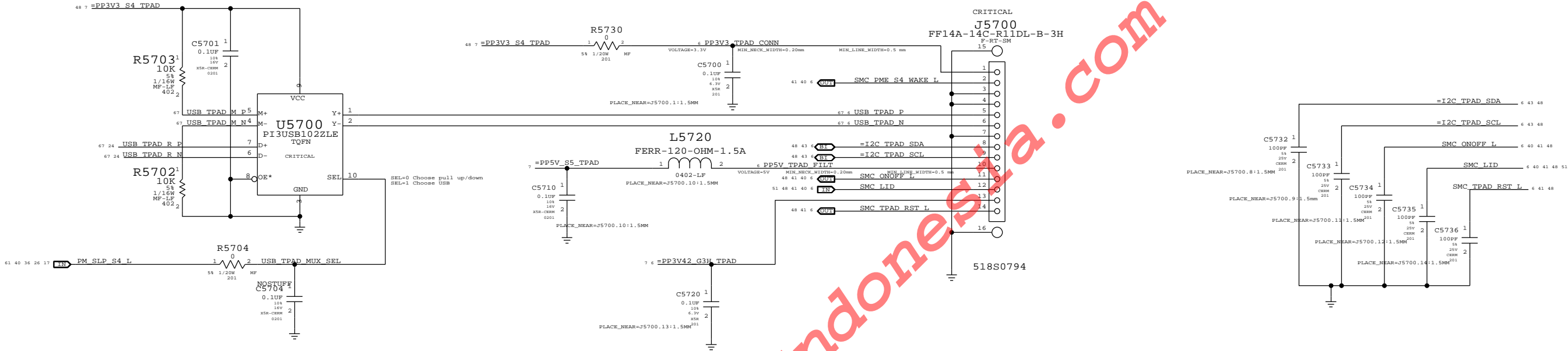
D

C

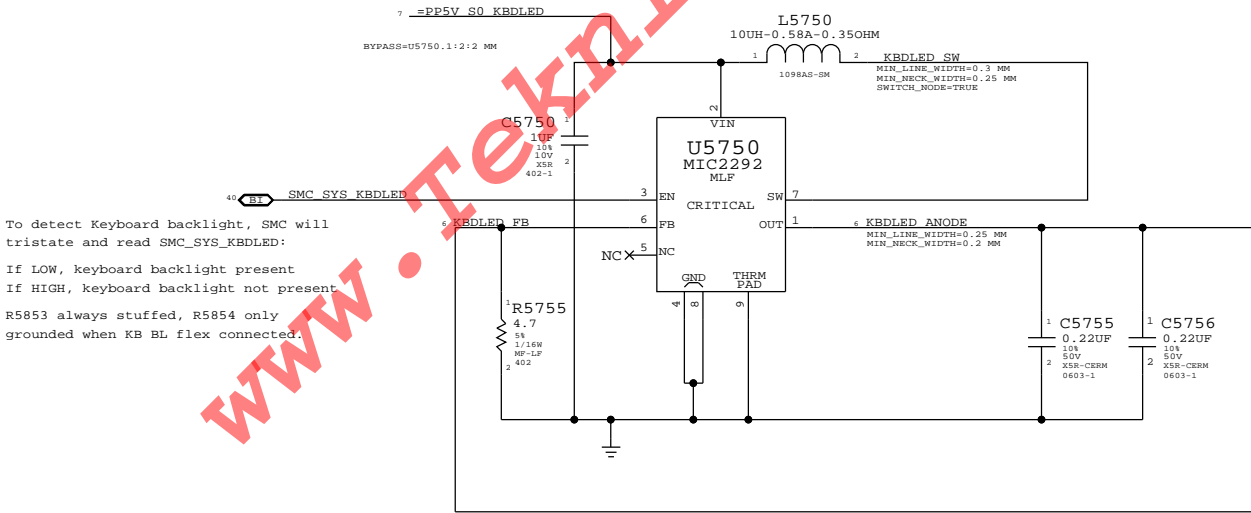
B

A

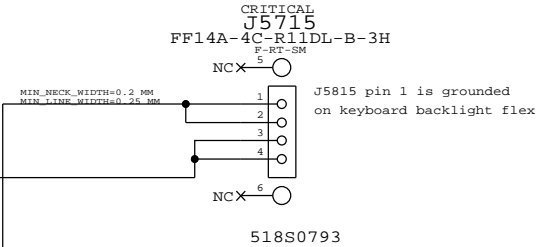
IPD Flex Connector




Keyboard Backlight Driver & Detection

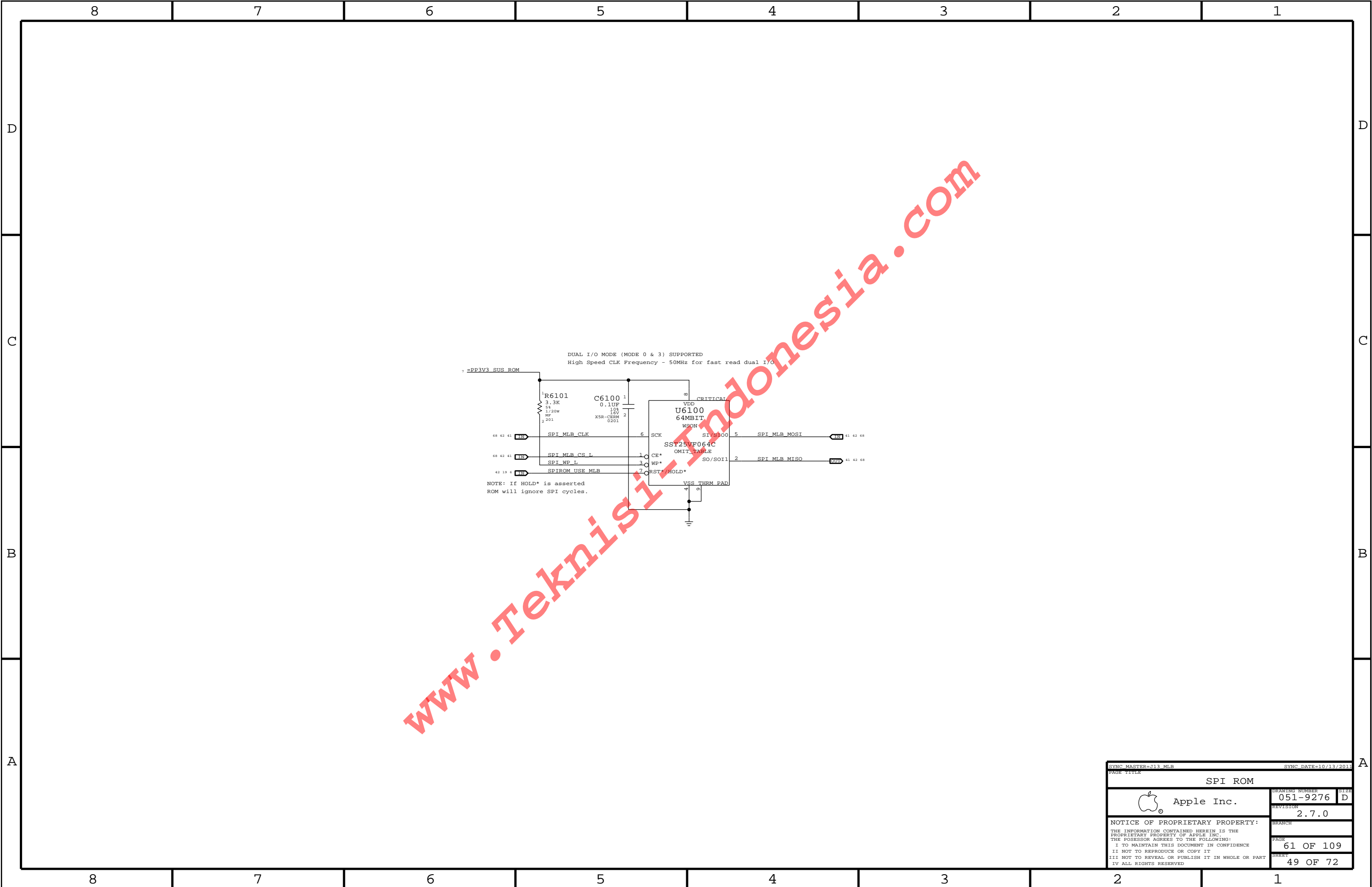


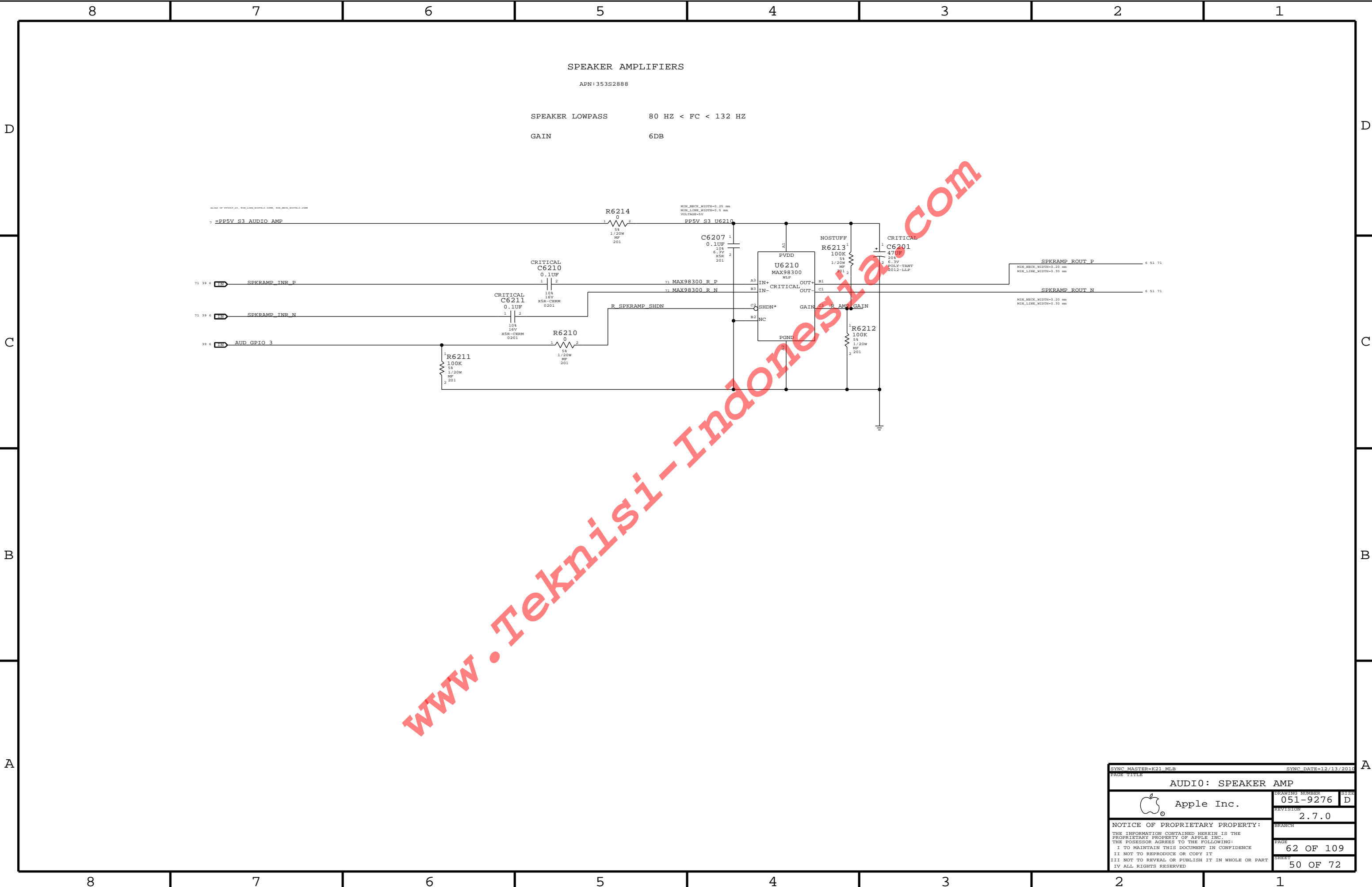
Keyboard Backlight Connector



SYNC MASTER=K21 MLB		SYNC DATE=12/13/2010	
PAGE TITLE			
IPD / KBD Backlight			
 Apple Inc.		DRAWING NUMBER	051-9276
		SIZE	D
		REVISION	2.7.0
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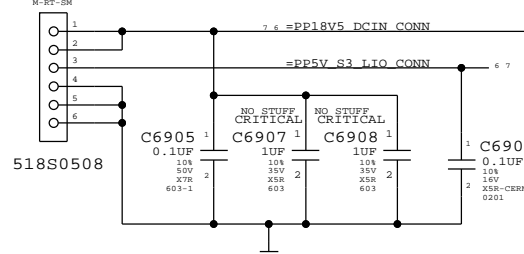






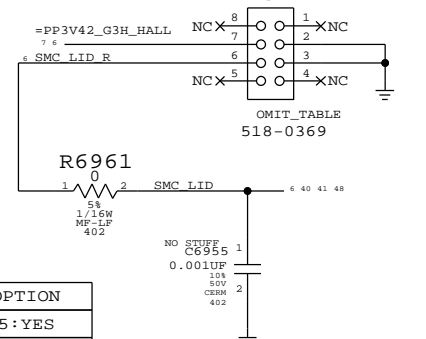
MLB to LIO Power Cable Connector

CRITICAL  
J6900  
WTB-PWR-M82  
M-RT-SM

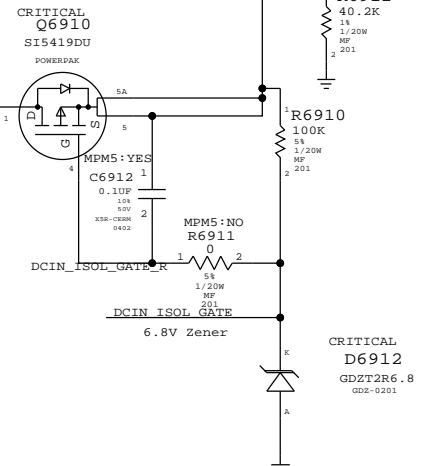
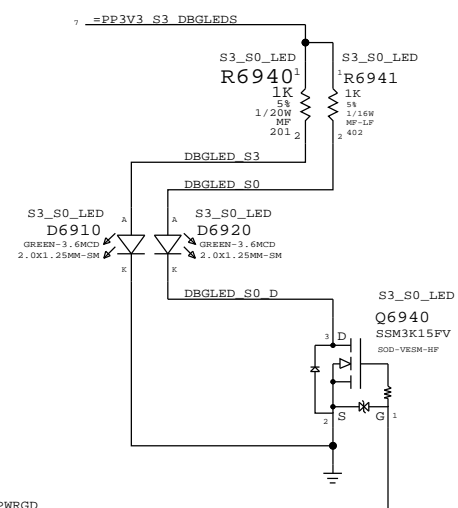


苹果笔记本维修交流群：325742634

J6955  
HALL-SENSOR-MLB-PADS-K99  
SM



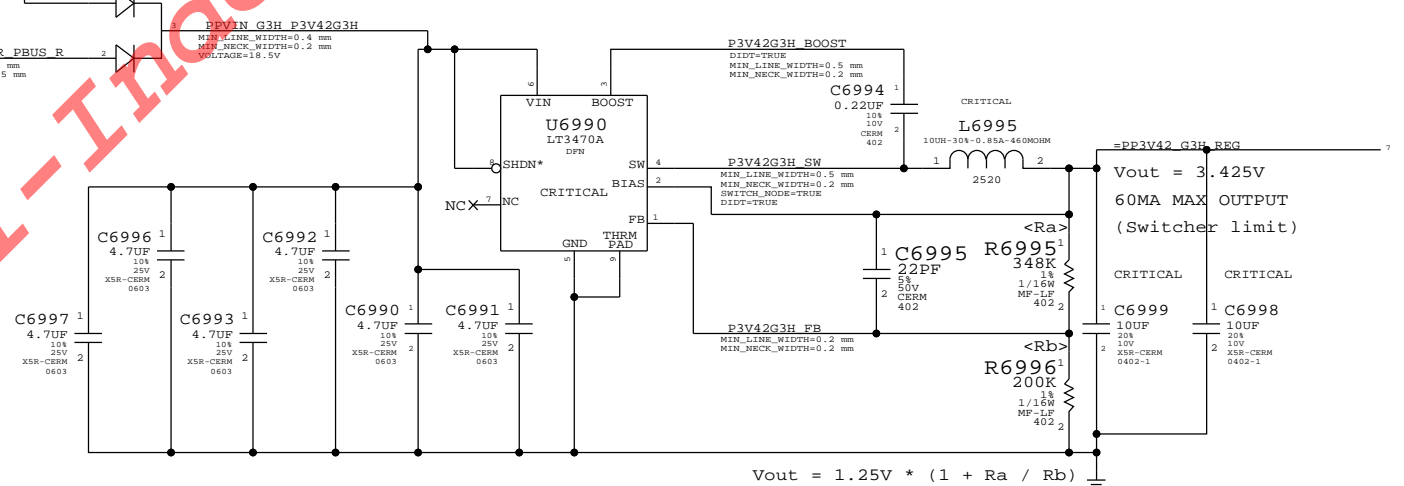
Debug LEDs  
(For development only)



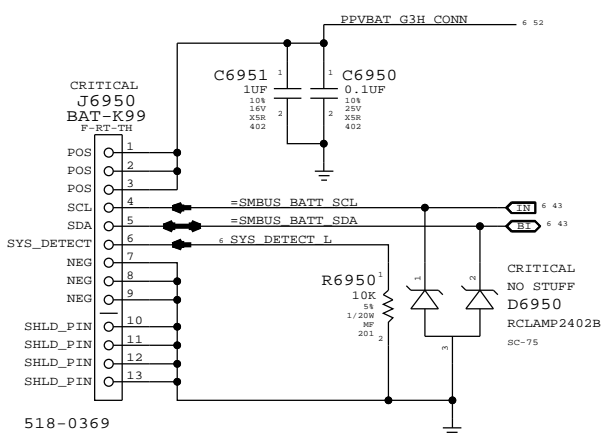
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0560	1	RES,MP,90.9KOHM,1,1/20W,0201	R6912	CRITICAL	MPMS:YES
117S0008	1	RES,MP,100KOHM,1,1/20W,0201	R6911	CRITICAL	MPMS:YES

3.425V "G3Hot" Supply

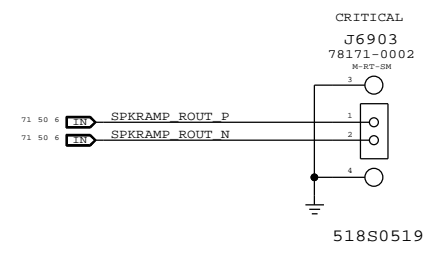
Supply needs to guarantee 3.1V delivered to SMC Vref generator



K99-Specific  
Battery Connector



Right Speaker Connector



SYMC PARTNERSHIP M82  
PAGE TITLE  
DC-In & Battery Connectors  
Apple Inc.  
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DRAWING NUMBER  
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SIZE  
D

Need to stuff R7092 if either PP5V5\_DCIN:YES or PP5V5\_VDDP are used!

### Reverse-Current Protection

### Inrush Limiter

5.5v "G3Hot" Supply  
For Erp Lot6 spec

PP5V5\_DCIN:YES

PP5V5\_VDDP

Vout = 5.50V  
200mA MAX OUTPUT  
(Switcher limit)

$$V_{out} = 1.25V * (1 + R_a / R_b)$$


Max Current = 8A

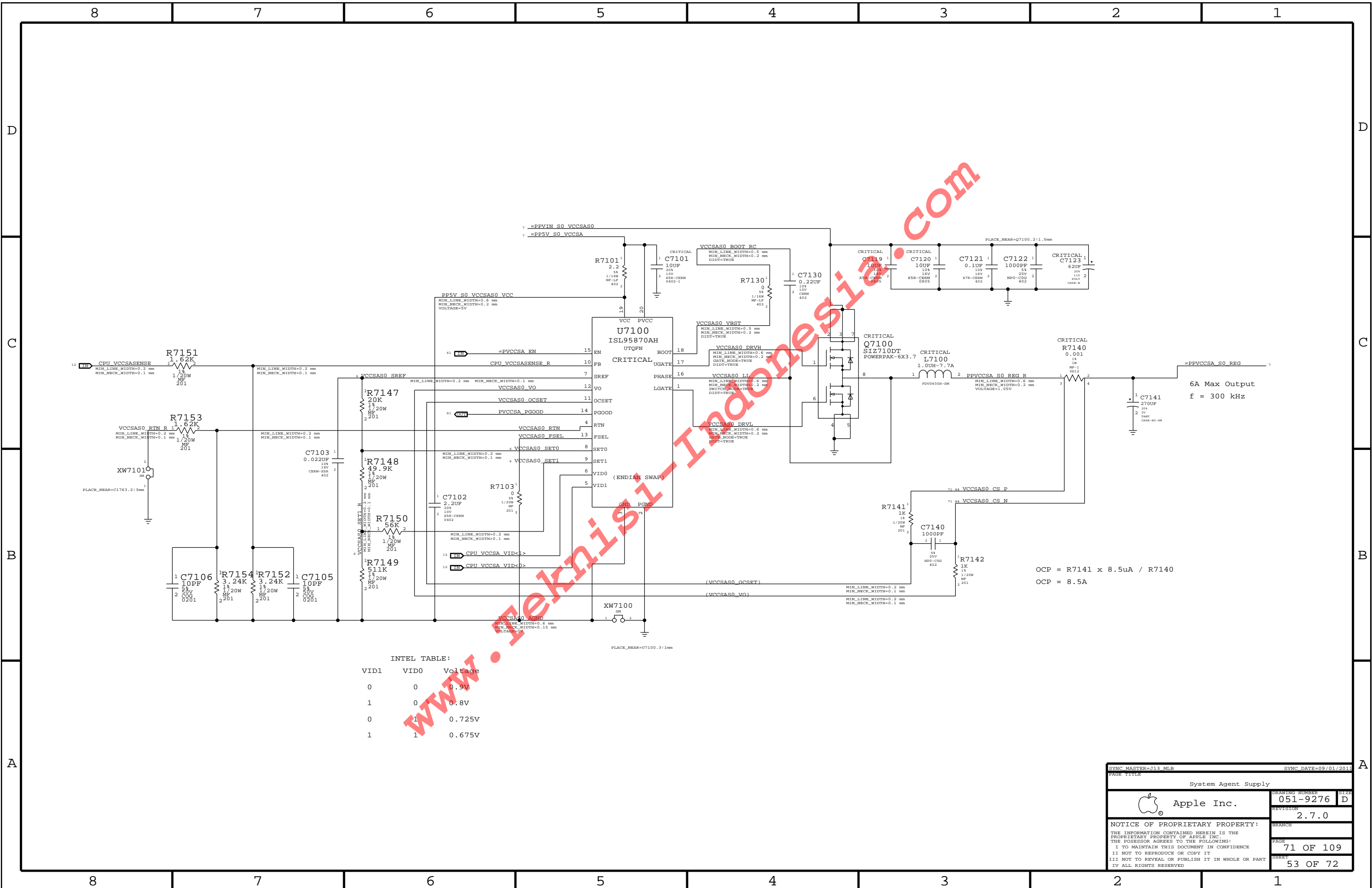
f = 400 kHz

TO SYSTEM

TO/FROM BATTERY

苹果笔记本维修交流群：325742634

SYNC MASTER=F13 MLB		SYNC DATE=10/10/2013	
PAGE TITLE			
PBus Supply & Battery Charger			
 Apple Inc.		DRAWING NUMBER	051-9276
		REVISION	2.7.0
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INTEL TABLE:


VID1	VID0	Voltage
0	0	0.9V
1	0	0.8V
0	1	0.725V
1	1	0.675V

$$OCP = R7141 \times 8.5\mu A / R7140$$
$$OCP = 8.5A$$

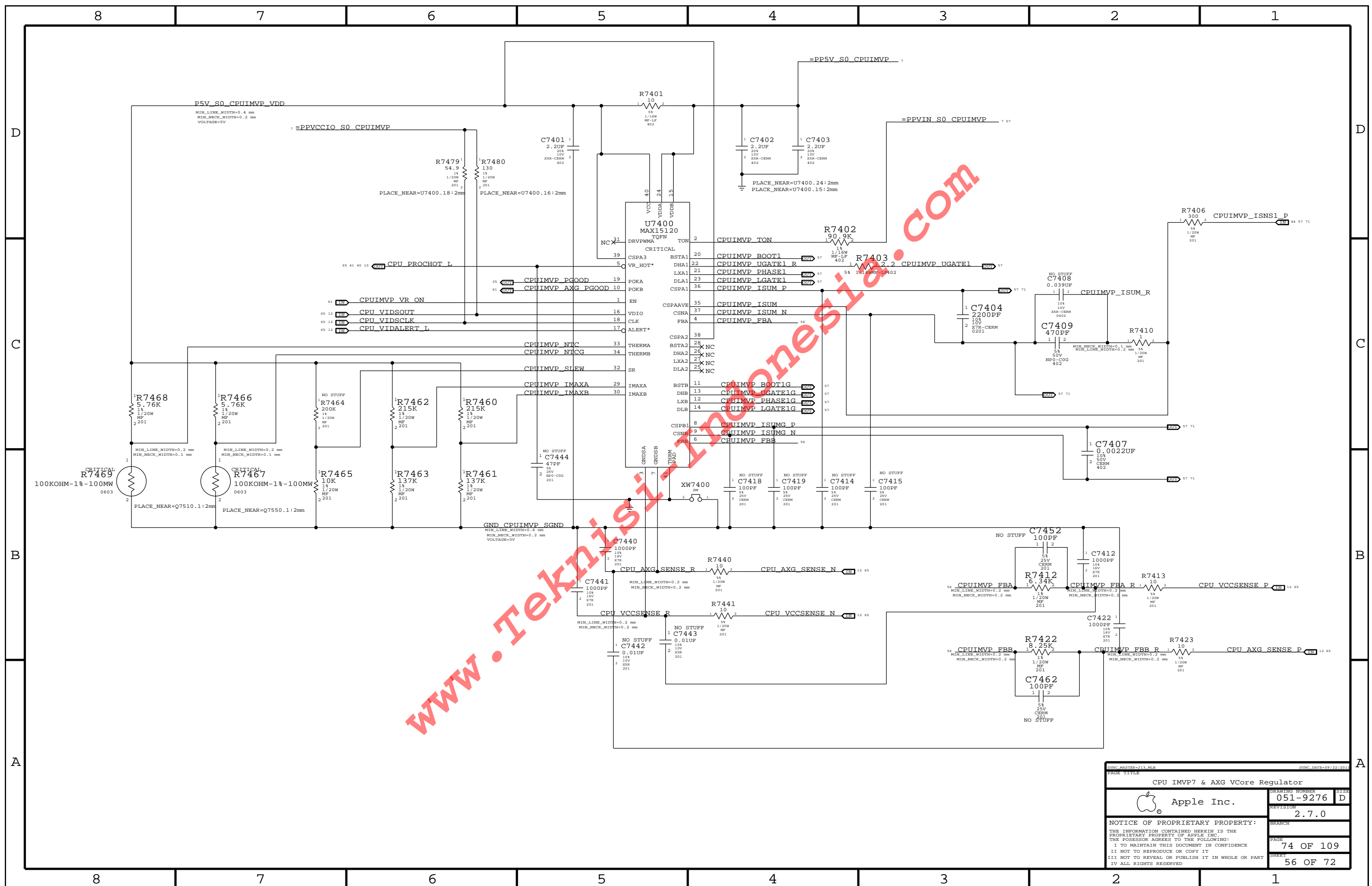


苹果笔记本维修交流群：325742634

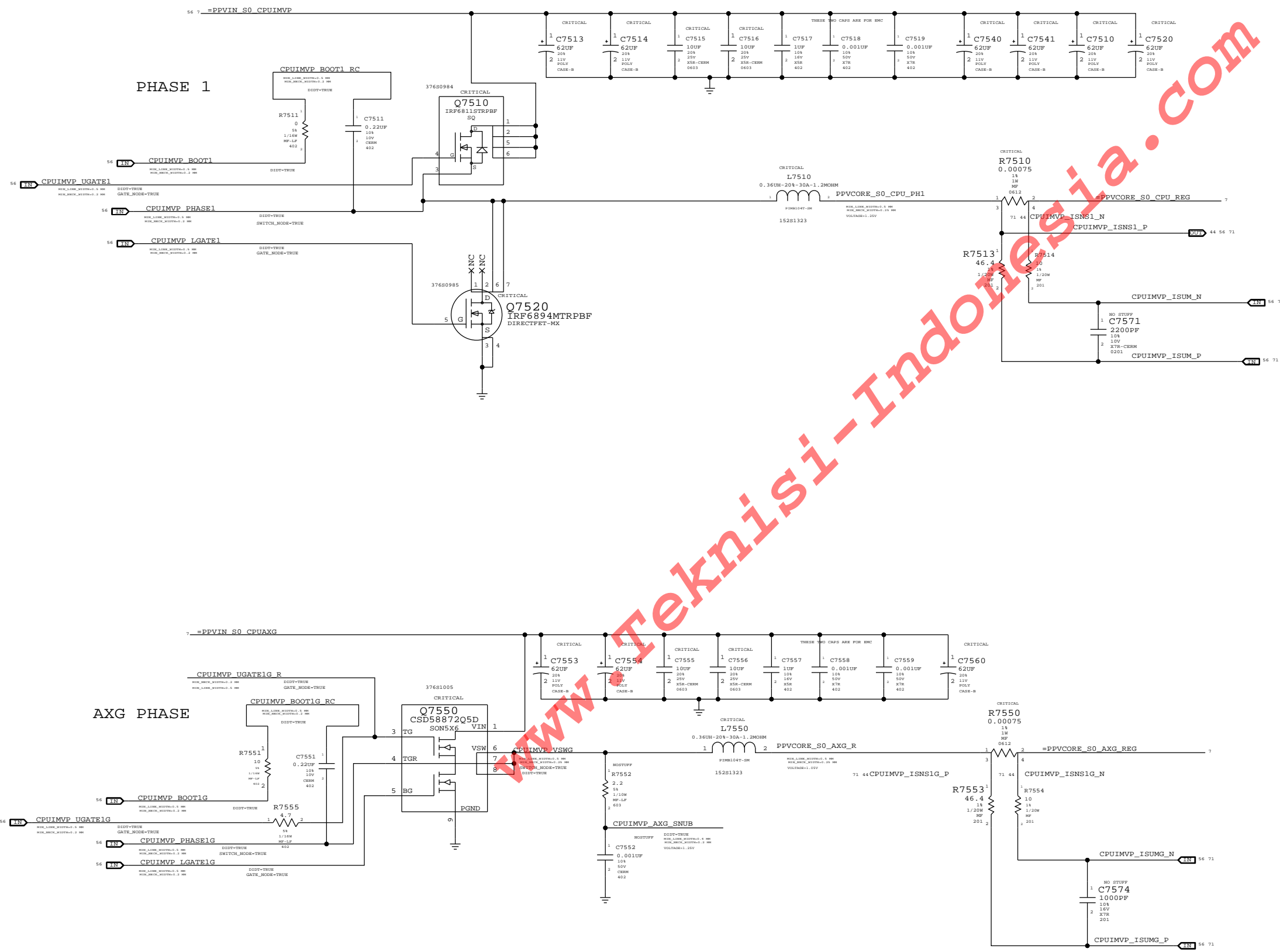
www.TeknisiIndonesia.com

SYNC MASTER=713 MLB		SYNC DATE=11/18/2011	
PAGE TITLE			
5V / 3.3V Power Supply			
 Apple Inc.	DRAWING NUMBER	051-9276	SIZE D
	REVISION	2.7.0	
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CPU=IV Bridge ULV, AXG=GT2

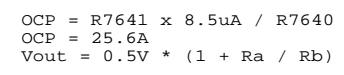


CPU IMVP7 & AXG VCore Output		
Apple Inc.		
DRAWING NUMBER	051-9276	SIZE D
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$$OCP = R7641 \times 8.5uA / R7640$$

$$OCP = 25.6A$$

$$Vout = 0.5V * (1 + Ra / Rb)$$





D

C

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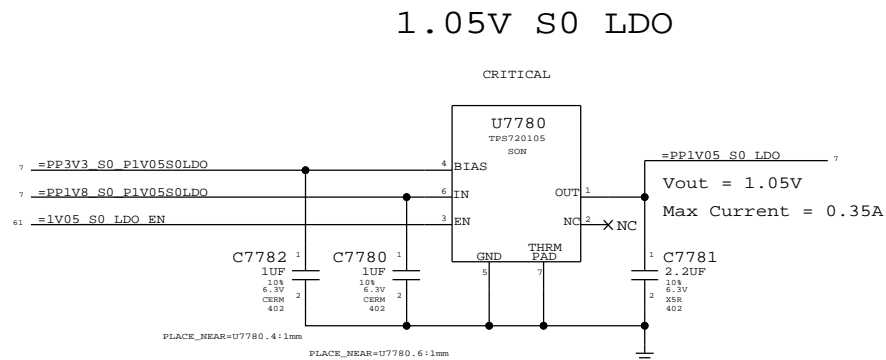
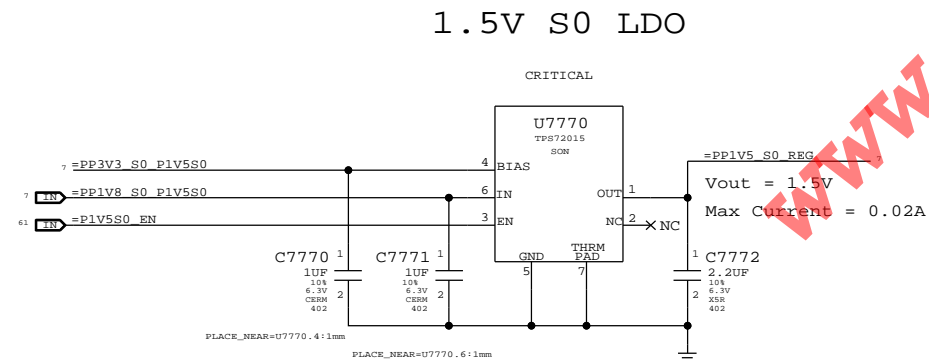
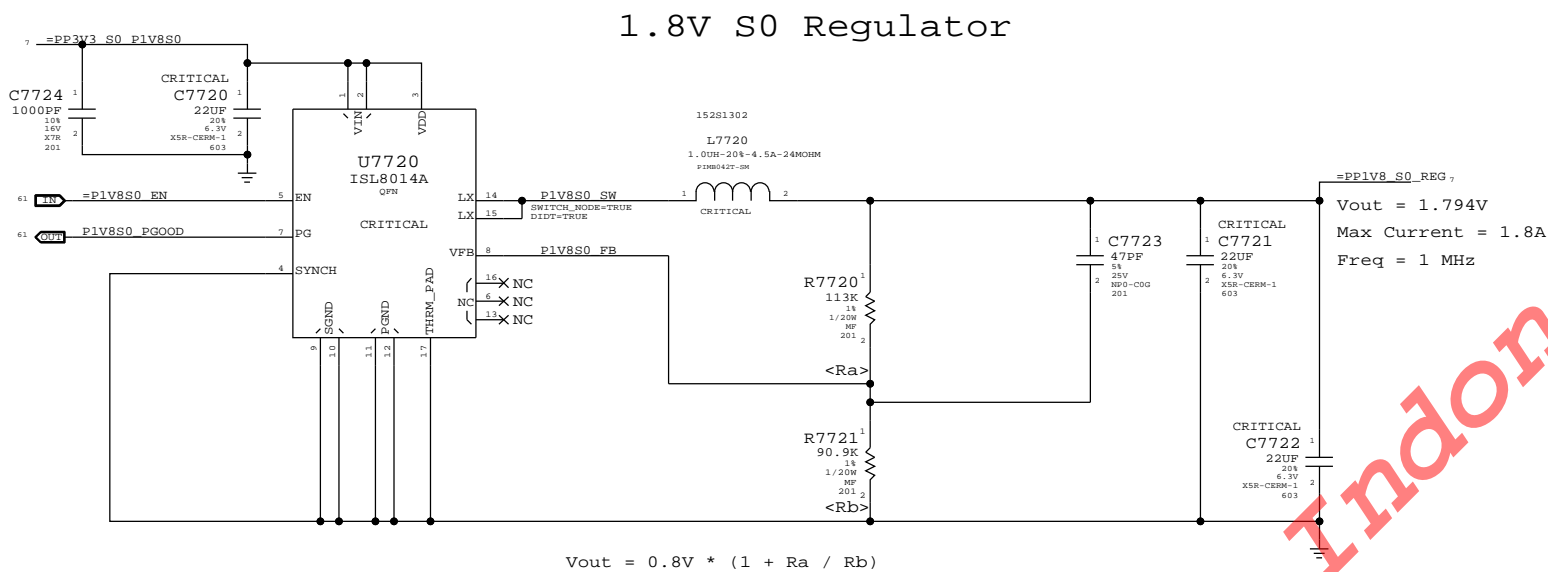
A

D

C

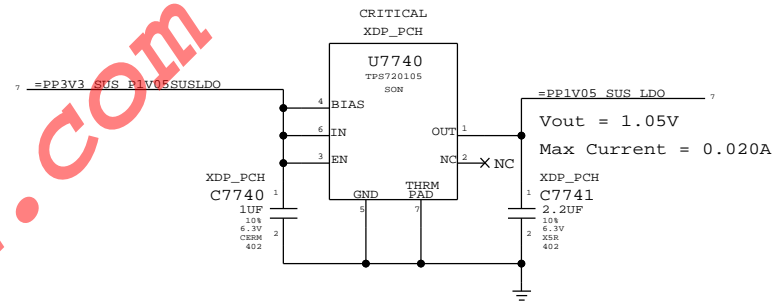
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
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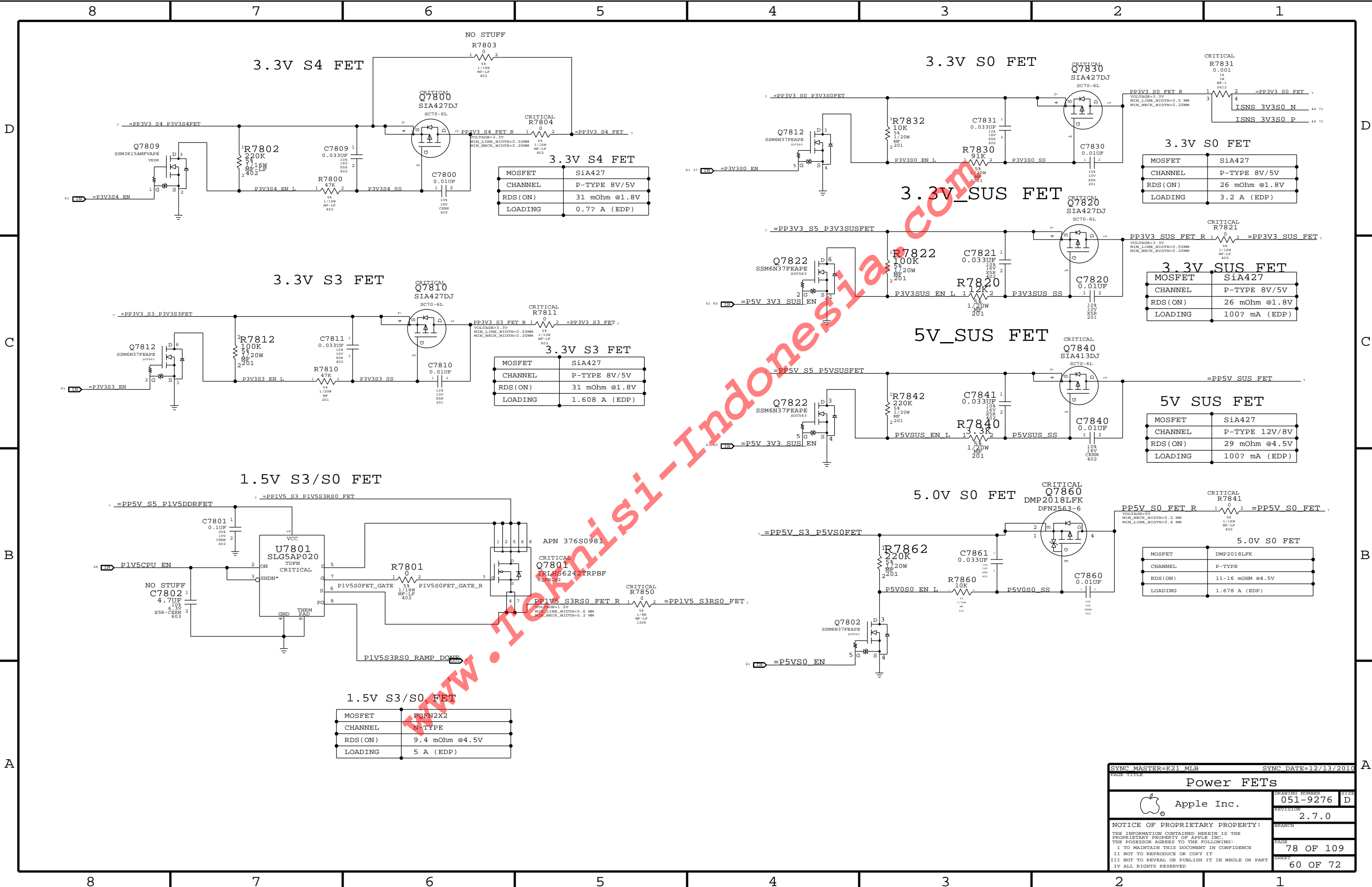


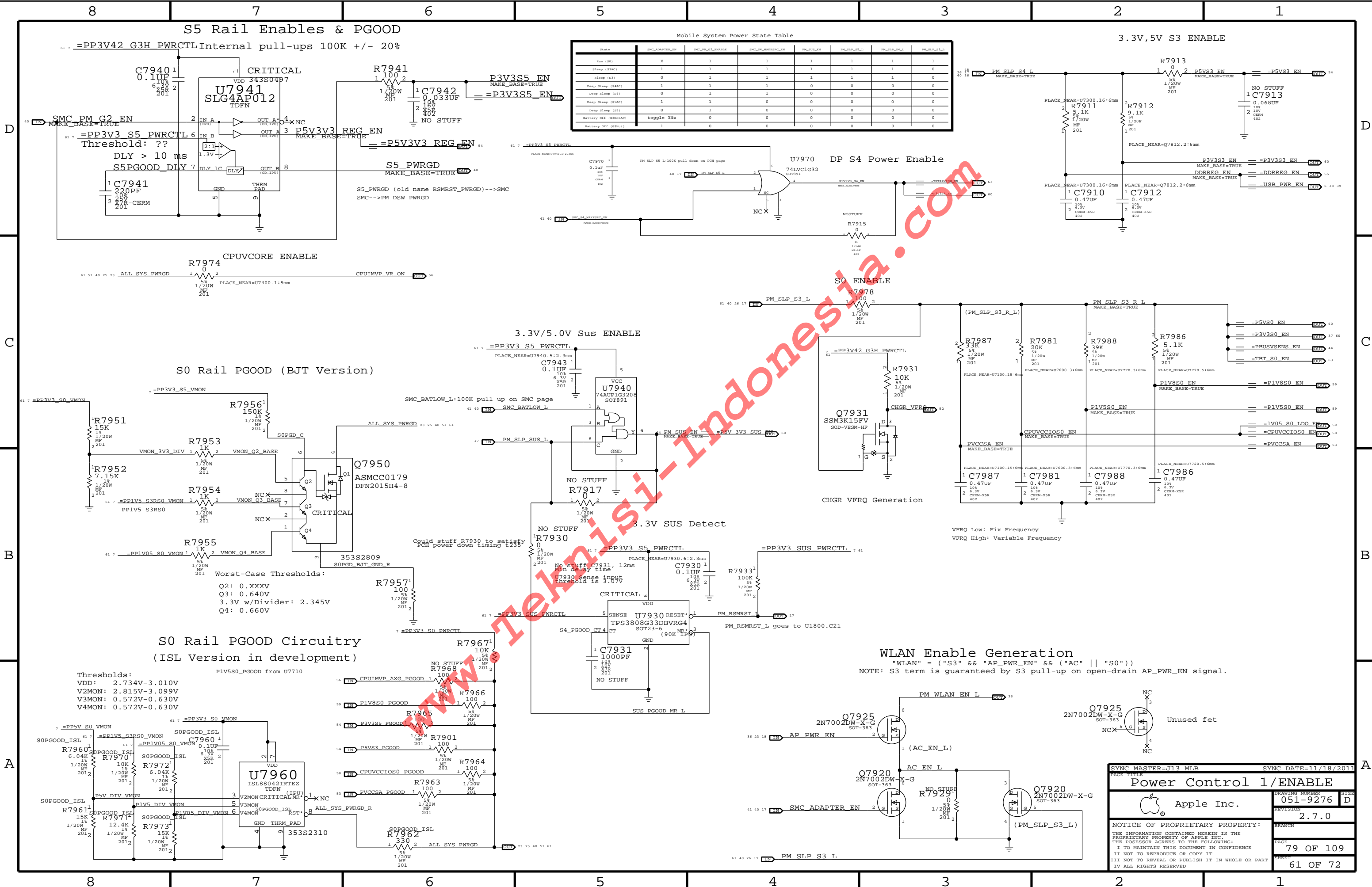
1.05V SUS LDO

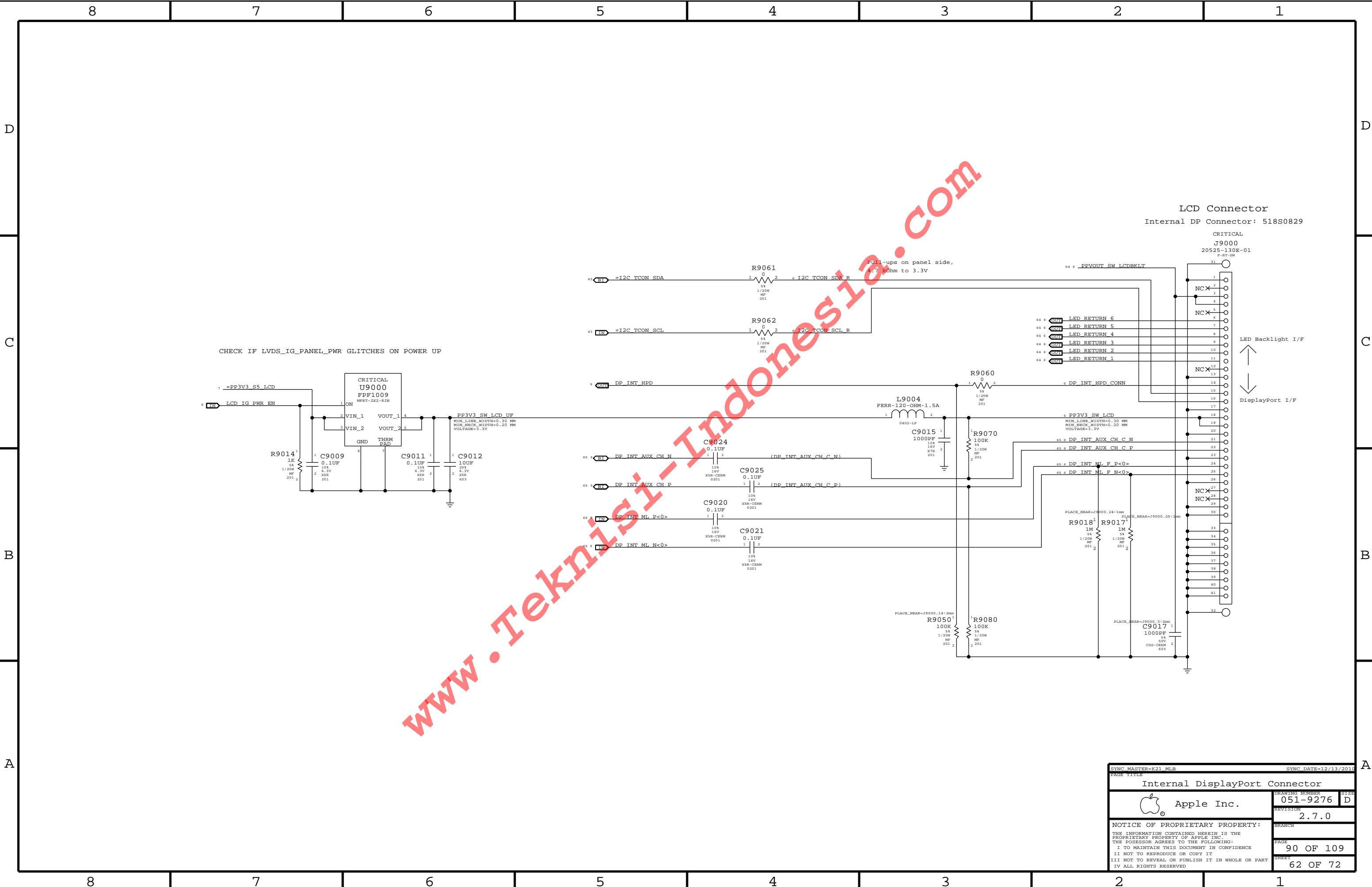
Cougar Point requires JTAG pull-ups to be powered at 1.05V when SUS suspend well is active. Pull-ups (3) must be 51 ohms to support XDP (not required in production). 70mA is required to support pull-ups. Alternative is strong voltage dividers (200/100) to 3.3V S5, which burns 100mW in all S-states.



SYNC MASTER-K21 MLB		SYNC DATE-12/13/2010	
PAGE TITLE			
Misc Power Supplies			
 Apple Inc.	DRAWING NUMBER		SIZE
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		2.7.0	
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SYNC MASTER=K21 MLB		SYNC DATE=12/13/2010	
PAGE TITLE			
Internal DisplayPort Connector			
 Apple Inc.	DRAWING NUMBER		SIZE
	051-9276		D
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8	7	6	5	4	3	2	1
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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0145	2	RES_MF,1/20W,17.8K,1,0201	R9410,R9413		TBTHV:P12V
118S0145	2	RES_MF,1/20W,17.8K,1,0201	R9411,R9414		TBTHV:P12V

B



8	7	6	5	4	3	2	1
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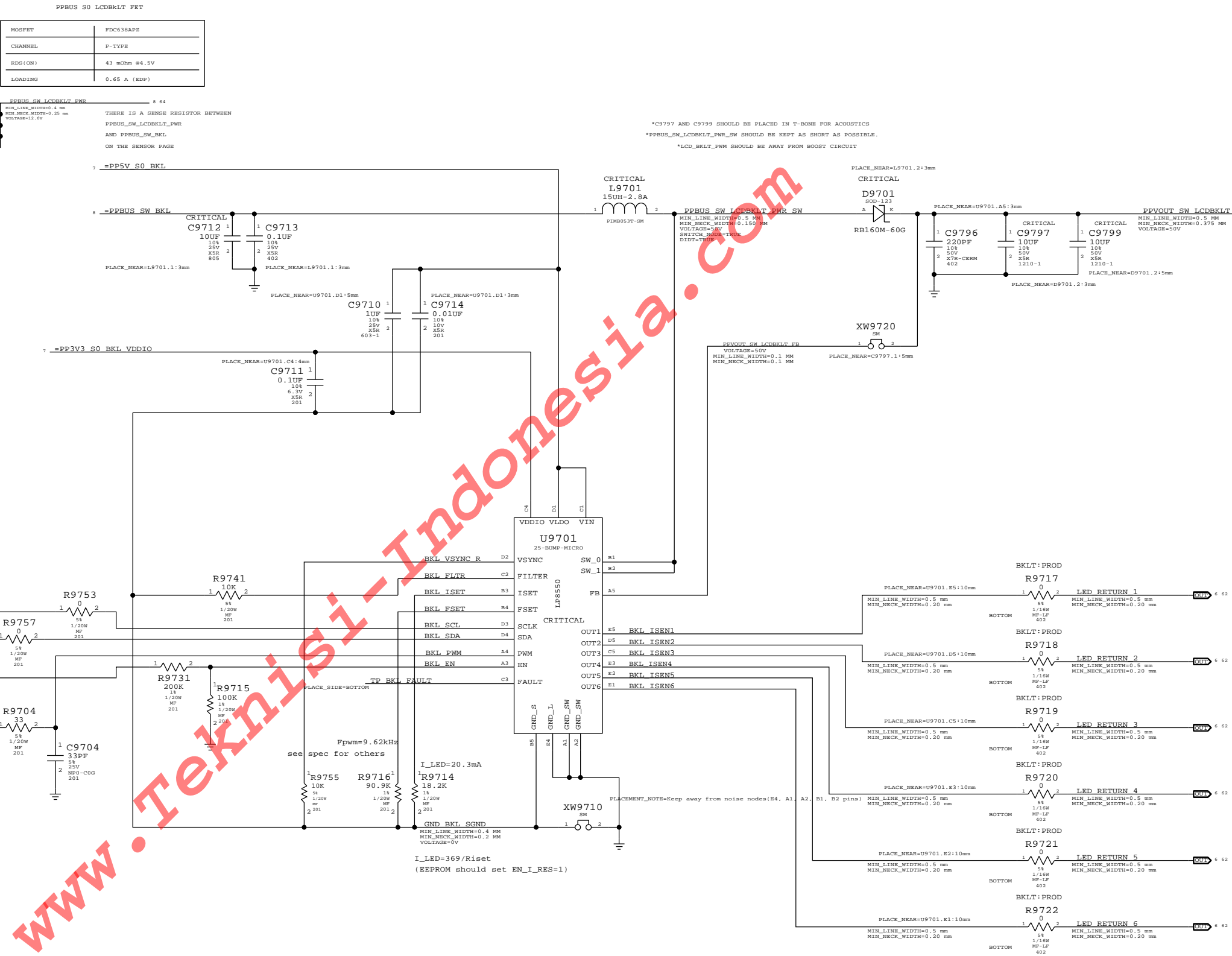
4	3	2	1
---	---	---	---



B

A





PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
103S0198	3	RES, THIN FILM, 1/16W, 10.2 OHM, 0.1, 0402, 0H	R9717, R9718, R9719		BKLT:ENG
103S0198	3	RES, THIN FILM, 1/16W, 10.2 OHM, 0.1, 0402, 0H	R9720, R9721, R9722		BKLT:ENG

10.2 ohm resistors for current measurement on LED strings.

SYNC MASTER=J13 MLB		SYNC DATE=10/13/2011	
PAGE TITLE			
LCD Backlight Driver			
DRAWING NUMBER		SIZE	
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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE
MEM_72D	*	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF
MEM_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_DATA2SELF	*	=2x_DIELECTRIC	?
MEM_DQS2OWNDATA	*	=3x_DIELECTRIC	?
MEM_CMD2CMD	*	=3x_DIELECTRIC	?
MEM_CMD2CTRL	*	=3x_DIELECTRIC	?
MEM_CTRL2CTRL	*	=3x_DIELECTRIC	?
MEM_CLK2CLK	*	=6x_DIELECTRIC	?
MEM_2OTHERMEM	*	=4x_DIELECTRIC	?
MEM_2PWR	*	=PWR_P2MM	?
MEM_2GND	*	=GND_P2MM	?
MEM_2OTHER	*	=6x_DIELECTRIC	?

PalPilot Spacing

=2x\_DIELECTRIC  
=5.7x\_DIELECTRIC  
=4x\_DIELECTRIC  
=4x\_DIELECTRIC  
=8.6x\_DIELECTRIC  
=5.7x\_DIELECTRIC  
=PWR\_P2MM  
=GND\_P2MM  
=8.6x\_DIELECTRIC

"Real" Spacing

=2x\_DIELECTRIC  
=3x\_DIELECTRIC  
=3x\_DIELECTRIC  
=3x\_DIELECTRIC  
=6x\_DIELECTRIC  
=4x\_DIELECTRIC  
=PWR\_P2MM  
=GND\_P2MM  
=6x\_DIELECTRIC

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_PWR	MEM_*	*	MEM_2PWR
MEM_PWR	*	*	DEFAULT

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	MEM_*	*	MEM_2GND

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DQS_0	MEM_A_DATA_0	*	MEM_DQS2OWNDATA
MEM_A_DQS_1	MEM_A_DATA_1	*	MEM_DQS2OWNDATA
MEM_A_DQS_2	MEM_A_DATA_2	*	MEM_DQS2OWNDATA
MEM_A_DQS_3	MEM_A_DATA_3	*	MEM_DQS2OWNDATA
MEM_A_DQS_4	MEM_A_DATA_4	*	MEM_DQS2OWNDATA
MEM_A_DQS_5	MEM_A_DATA_5	*	MEM_DQS2OWNDATA
MEM_A_DQS_6	MEM_A_DATA_6	*	MEM_DQS2OWNDATA
MEM_A_DQS_7	MEM_A_DATA_7	*	MEM_DQS2OWNDATA
MEM_B_DQS_0	MEM_B_DATA_0	*	MEM_DQS2OWNDATA
MEM_B_DQS_1	MEM_B_DATA_1	*	MEM_DQS2OWNDATA
MEM_B_DQS_2	MEM_B_DATA_2	*	MEM_DQS2OWNDATA
MEM_B_DQS_3	MEM_B_DATA_3	*	MEM_DQS2OWNDATA
MEM_B_DQS_4	MEM_B_DATA_4	*	MEM_DQS2OWNDATA
MEM_B_DQS_5	MEM_B_DATA_5	*	MEM_DQS2OWNDATA
MEM_B_DQS_6	MEM_B_DATA_6	*	MEM_DQS2OWNDATA
MEM_B_DQS_7	MEM_B_DATA_7	*	MEM_DQS2OWNDATA

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DATA_*	=SAME	*	MEM_DATA2SELF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_CTRL	*	MEM_CMD2CTRL
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2CLK

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*	MEM_*	*	MEM_2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DQS_0	*	*	MEM_2OTHER
MEM_A_DQS_1	*	*	MEM_2OTHER
MEM_A_DQS_2	*	*	MEM_2OTHER
MEM_A_DQS_3	*	*	MEM_2OTHER
MEM_A_DQS_4	*	*	MEM_2OTHER
MEM_A_DQS_5	*	*	MEM_2OTHER
MEM_A_DQS_6	*	*	MEM_2OTHER
MEM_A_DQS_7	*	*	MEM_2OTHER
MEM_B_DQS_0	*	*	MEM_2OTHER
MEM_B_DQS_1	*	*	MEM_2OTHER
MEM_B_DQS_2	*	*	MEM_2OTHER
MEM_B_DQS_3	*	*	MEM_2OTHER
MEM_B_DQS_4	*	*	MEM_2OTHER
MEM_B_DQS_5	*	*	MEM_2OTHER
MEM_B_DQS_6	*	*	MEM_2OTHER
MEM_B_DQS_7	*	*	MEM_2OTHER

MEM_A_DATA_0	*	*	MEM_2OTHER
MEM_A_DATA_1	*	*	MEM_2OTHER
MEM_A_DATA_2	*	*	MEM_2OTHER
MEM_A_DATA_3	*	*	MEM_2OTHER
MEM_A_DATA_4	*	*	MEM_2OTHER
MEM_A_DATA_5	*	*	MEM_2OTHER
MEM_A_DATA_6	*	*	MEM_2OTHER
MEM_A_DATA_7	*	*	MEM_2OTHER

MEM_B_DATA_0	*	*	MEM_2OTHER
MEM_B_DATA_1	*	*	MEM_2OTHER
MEM_B_DATA_2	*	*	MEM_2OTHER
MEM_B_DATA_3	*	*	MEM_2OTHER
MEM_B_DATA_4	*	*	MEM_2OTHER
MEM_B_DATA_5	*	*	MEM_2OTHER
MEM_B_DATA_6	*	*	MEM_2OTHER
MEM_B_DATA_7	*	*	MEM_2OTHER

MEM_CMD	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CLK	*	*	MEM_2OTHER

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
MEM_A_CLK	MEM_72D	MEM_CLK	MEM A CLK P<5..0>	8 11 27 28 32
MEM_A_CLK	MEM_72D	MEM_CLK	MEM A CLK N<5..0>	8 11 27 28 32
MEM_A_CTRL	MEM_45S	MEM_CTRL	MEM A CKE<3..0>	11 27 28 32
MEM_A_CTRL	MEM_45S	MEM_CTRL	MEM A CS L<3..0>	11 27 28 32
MEM_A_CTRL	MEM_45S	MEM_CTRL	MEM A ODT<3..0>	11 27 28 32
MEM_A_CMD	MEM_45S	MEM_CMD	MEM A A<15..0>	11 27 28 32
MEM_A_CMD	MEM_45S	MEM_CMD	MEM A BA<2..0>	11 27 28 32
MEM_A_CMD	MEM_45S	MEM_CMD	MEM A RAS L	11 27 28 32
MEM_A_CMD	MEM_45S	MEM_CMD	MEM A CAS L	11 27 28 32
MEM_A_CMD	MEM_45S	MEM_CMD	MEM A WE L	11 27 28 32
MEM_A_DQ_BYTE0	MEM_45S	MEM_A_DATA_0	MEM A DQ<7..0>	11 27
MEM_A_DQ_BYTE1	MEM_45S	MEM_A_DATA_1	MEM A DQ<15..8>	11 27
MEM_A_DQ_BYTE2	MEM_45S	MEM_A_DATA_2	MEM A DQ<23..16>	11 27
MEM_A_DQ_BYTE3	MEM_45S	MEM_A_DATA_3	MEM A DQ<31..24>	11 27
MEM_A_DQ_BYTE4	MEM_45S	MEM_A_DATA_4	MEM A DQ<39..32>	11 28
MEM_A_DQ_BYTE5	MEM_45S	MEM_A_DATA_5	MEM A DQ<47..40>	11 28
MEM_A_DQ_BYTE6	MEM_45S	MEM_A_DATA_6	MEM A DQ<55..48>	11 28
MEM_A_DQ_BYTE7	MEM_45S	MEM_A_DATA_7	MEM A DQ<63..56>	11 28
MEM_A_DQS0	MEM_80D	MEM_A_DQS_0	MEM A DOS P<0>	11 27
MEM_A_DQS0	MEM_80D	MEM_A_DQS_0	MEM A DOS N<0>	11 27
MEM_A_DQS1	MEM_80D	MEM_A_DQS_1	MEM A DOS P<1>	11 27
MEM_A_DQS1	MEM_80D	MEM_A_DQS_1	MEM A DOS N<1>	11 27
MEM_A_DQS2	MEM_80D	MEM_A_DQS_2	MEM A DOS P<2>	11 27
MEM_A_DQS2	MEM_80D	MEM_A_DQS_2	MEM A DOS N<2>	11 27
MEM_A_DQS3	MEM_80D	MEM_A_DQS_3	MEM A DOS P<3>	11 27
MEM_A_DQS3	MEM_80D	MEM_A_DQS_3	MEM A DOS N<3>	11 27
MEM_A_DQS4	MEM_80D	MEM_A_DQS_4	MEM A DOS P<4>	11 28
MEM_A_DQS4	MEM_80D	MEM_A_DQS_4	MEM A DOS N<4>	11 28
MEM_A_DQS5	MEM_80D	MEM_A_DQS_5	MEM A DOS P<5>	11 28
MEM_A_DQS5	MEM_80D	MEM_A_DQS_5	MEM A DOS N<5>	11 28
MEM_A_DQS6	MEM_80D	MEM_A_DQS_6	MEM A DOS P<6>	11 28
MEM_A_DQS6	MEM_80D	MEM_A_DQS_6	MEM A DOS N<6>	11 28
MEM_A_DQS7	MEM_80D	MEM_A_DQS_7	MEM A DOS P<7>	11 28
MEM_A_DQS7	MEM_80D	MEM_A_DQS_7	MEM A DOS N<7>	11 28
MEM_B_CLK	MEM_72D	MEM_CLK	MEM B CLK P<5..0>	8 11 29 30 32
MEM_B_CLK	MEM_72D	MEM_CLK	MEM B CLK N<5..0>	8 11 29 30 32
MEM_B_CTRL	MEM_45S	MEM_CTRL	MEM B CKE<3..0>	11 29 30 32
MEM_B_CTRL	MEM_45S	MEM_CTRL	MEM B CS L<3..0>	11 29 30 32
MEM_B_CTRL	MEM_45S	MEM_CTRL	MEM B ODT<3..0>	11 29 30 32
MEM_B_CMD	MEM_45S	MEM_CMD	MEM B A<15..0>	11 29 30 32
MEM_B_CMD	MEM_45S	MEM_CMD	MEM B BA<2..0>	11 29 30 32
MEM_B_CMD	MEM_45S	MEM_CMD	MEM B RAS L	11 29 30 32
MEM_B_CMD	MEM_45S	MEM_CMD	MEM B CAS L	11 29 30 32
MEM_B_CMD	MEM_45S	MEM_CMD	MEM B WE L	11 29 30 32
MEM_B_DQ_BYTE0	MEM_45S	MEM_B_DATA_0	MEM B DQ<7..0>	11 29
MEM_B_DQ_BYTE1	MEM_45S	MEM_B_DATA_1	MEM B DQ<15..8>	11 29
MEM_B_DQ_BYTE2	MEM_45S	MEM_B_DATA_2	MEM B DQ<23..16>	11 29
MEM_B_DQ_BYTE3	MEM_45S	MEM_B_DATA_3	MEM B DQ<31..24>	11 30
MEM_B_DQ_BYTE4	MEM_45S	MEM_B_DATA_4	MEM B DQ<39..32>	11 30
MEM_B_DQ_BYTE5	MEM_45S	MEM_B_DATA_5	MEM B DQ<47..40>	11 30
MEM_B_DQ_BYTE6	MEM_45S	MEM_B_DATA_6	MEM B DQ<55..48>	11 30
MEM_B_DQ_BYTE7	MEM_45S	MEM_B_DATA_7	MEM B DQ<63..56>	11 30
MEM_B_DQS0	MEM_80D	MEM_B_DQS_0	MEM B DOS P<0>	11 29
MEM_B_DQS0	MEM_80D	MEM_B_DQS_0	MEM B DOS N<0>	11 29
MEM_B_DQS1	MEM_80D	MEM_B_DQS_1	MEM B DOS P<1>	11 29
MEM_B_DQS1	MEM_80D	MEM_B_DQS_1	MEM B DOS N<1>	11 29
MEM_B_DQS2	MEM_80D	MEM_B_DQS_2	MEM B DOS P<2>	11 29
MEM_B_DQS2	MEM_80D	MEM_B_DQS_2	MEM B DOS N<2>	11 29
MEM_B_DQS3	MEM_80D	MEM_B_DQS_3	MEM B DOS P<3>	11 29
MEM_B_DQS3	MEM_80D	MEM_B_DQS_3	MEM B DOS N<3>	11 29
MEM_B_DQS4	MEM_80D	MEM_B_DQS_4	MEM B DOS P<4>	11 30
MEM_B_DQS4	MEM_80D	MEM_B_DQS_4	MEM B DOS N<4>	11 30
MEM_B_DQS5	MEM_80D	MEM_B_DQS_5	MEM B DOS P<5>	11 30
MEM_B_DQS5	MEM_80D	MEM_B_DQS_5	MEM B DOS N<5>	11 30
MEM_B_DQS6	MEM_80D	MEM_B_DQS_6	MEM B DOS P<6>	11 30
MEM_B_DQS6	MEM_80D	MEM_B_DQS_6	MEM B DOS N<6>	11 30
MEM_B_DQS7	MEM_80D	MEM_B_DQS_7	MEM B DOS P<7>	11 30
MEM_B_DQS7	MEM_80D	MEM_B_DQS_7	MEM B DOS N<7>	11 30
		MEM_PWR	PP1V5 S3RS0	6 7
		MEM_PWR	PP1V5 S3	6 7
		MEM_PWR	PP0V75 S3 MEM VREFCA A	27 28 31
		MEM_PWR	PP0V75 S3 MEM VREFDO A	27 28 31





## LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	=3x_DIELECTRIC	?
CLK_LPC	*	=4x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905\_v1.5), Section 3.15

## SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_45S_R_50S	TOP,BOTTOM	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE		
SMB_45S_R_50S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

## HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFFAIR PRIMARY GAP	DIFFFAIR NECK GAP
HDA_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905\_v1.5), Section 3.15

## SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=4x_DIELECTRIC	?

## SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	=4x_DIELECTRIC	?

## XDP Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCH_ITP	*	=2:1_SPACING	?

## DisplayPort

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_2DP	*	=3x_DIELECTRIC	?	DP_2DP	TOP,BOTTOM	=4x_DIELECTRIC	?
DP_20THERHS	*	=4x_DIELECTRIC	?	DP_20THERHS	TOP,BOTTOM	=6x_DIELECTRIC	?
DP_20THER	*	=3x_DIELECTRIC	?	DP_20THER	TOP,BOTTOM	=4x_DIELECTRIC	?
DP_AUX	*	=3x_DIELECTRIC	?	DP_AUX	TOP,BOTTOM	=4x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DP_TX	DP_TX	*	DP_2DP
DP_TX	*_TX	*	DP_2OTHERHS
DP_TX	*_RX	*	DP_2OTHERHS
DP_TX	*	*	DP_2OTHER

## System Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_25M_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

















SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=2x_DIELECTRIC	?
CLK_25M	*	=5x_DIELECTRIC	?

NOTE: 25MHz system clocks very sensitive to noise.









## PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
LPC_AD	LPC_45S	LPC	LPC AD<3..0>	6 16 40
LPC_FRAME_L	LPC_45S	LPC	LPC FRAME_L	6 16 40 42
LPC_CLK33M	LPC_45S	LPC	LPCPLUS RESET_L	6 25 42
LPC_CLK33M	CLK_LPC_45S	CLK_LPC	LPC CLK33M SMC	25 40
LPC_CLK33M	CLK_LPC_45S	CLK_LPC	LPC CLK33M SMC R	18 25
LPC_CLK33M	CLK_LPC_45S	CLK_LPC	LPC CLK33M LPCPLUS	6 25 42
LPC_CLK33M	CLK_LPC_45S	CLK_LPC	LPC CLK33M LPCPLUS_R	18 25
LPC_CLK33M	CLK_LPC_45S	CLK_LPC	PCH CLK33M PCIIN	16 25
LPC_CLK33M	CLK_LPC_45S	CLK_LPC	PCH CLK33M PCIOUT	18 25
SMBUS_PCH_CLK	SMB_45S_P_50S	SMB	SMBUS PCH CLK	16 43
SMBUS_PCH_DATA	SMB_45S_R_50S	SMB	SMBUS PCH DATA	16 43
SMBUS_PCH_0_CLK	SMB_45S_R_50S	SMB	SML PCH 0 CLK	16 43
SMBUS_PCH_0_DATA	SMB_45S_P_50S	SMB	SML PCH 0 DATA	16 43
SMBUS_SMC_1_S0_SCT	SMB_45S_P_50S	SMB	SML PCH 1 CLK	16 43
SMBUS_SMC_1_S0_SDA	SMB_45S_R_50S	SMB	SML PCH 1 DATA	16 43
HDA_BIT_CLK	HDA_45S	HDA	HDA BIT CLK	6 16 39
HDA_SYNC	HDA_45S	HDA	HDA BIT CLK R	16
HDA_RST_L	HDA_45S	HDA	HDA SYNC	6 16 39
HDA_SDIN0	HDA_45S	HDA	HDA SYNC R	16
HDA_SDOUT	HDA_45S	HDA	HDA RST R L	6 16 39
HDA_SDOUT	HDA_45S	HDA	HDA SDIN0	6 16 39
HDA_SDOUT	HDA_45S	HDA	HDA SDOUT	6 16 39
HDA_SDOUT	HDA_45S	HDA	HDA SDOUT_R	16 25
PM_SUS_CLK	CLK_SLOW_45S	CLK_SLOW	PM_CLK32K SUSCLK_R	17 41
SEI_CLK	CLK_SLOW_45S	CLK_SLOW	SMC CLK32K	40 41
SEI_CLK	SPI_45S	SPI	SPI CLK_R	16 42
SEI_MOST	SPI_45S	SPI	SPI CLK	42
SEI_MISO	SPI_45S	SPI	SPI MOSI_R	16 42
SEI_CS0	SPI_45S	SPI	SPI MOSI	42
SEI_CS0	SPI_45S	SPI	SPI MISO	16 42
SEI_CS0	SPI_45S	SPI	SPI CS0_R_L	16 42
SEI_CS0	SPI_45S	SPI	SPI CS0_L	42
SEI_CS0	SPI_45S	SPI	SPI SMC CLK	40 41
SEI_CS0	SPI_45S	SPI	SPI SMC MOSI	40 41
SEI_CS0	SPI_45S	SPI	SPI SMC MISO	40 41
SEI_CS0	SPI_45S	SPI	SPI SMC CS_L	40 41
SEI_CS0	SPI_45S	SPI	SPI MLB CLK	41 42 49
SEI_CS0	SPI_45S	SPI	SPI MLB MOSI	41 42 49
SEI_CS0	SPI_45S	SPI	SPI MLB MISO	41 42 49
SEI_CS0	SPI_45S	SPI	SPI MLB CS_L	41 42 49
PCIE_AP_R2D	PCIE_80D	PCIE_PCH_TX	PCIE AP_R2D_P	6 36
PCIE_AP_R2D	PCIE_80D	PCIE_PCH_TX	PCIE AP_R2D_N	6 36
PCIE_AP_R2D	PCIE_80D	PCIE_PCH_TX	PCIE AP_R2D_C_P	16 36
PCIE_AP_R2D	PCIE_80D	PCIE_PCH_TX	PCIE AP_R2D_C_N	16 36
PCIE_AP_D2R	PCIE_80D	PCIE_PCH_RX	PCIE AP_R2D_R	6 16 36
PCIE_AP_D2R	PCIE_80D	PCIE_PCH_RX	PCIE AP_D2R_N	6 16 36
PCIE_CLK100M_AP	CLK_PCIE_80D	CLK_PCIE	PCIE CLK100M_AP_P	6 16 36
PCIE_CLK100M_AP	CLK_PCIE_80D	CLK_PCIE	PCIE CLK100M_AP_N	6 16 36
PCIE_TBT_R2D	PCIE_80D	PCIE_PCH_TX	PCIE TBT_R2D_P<3..0>	33
PCIE_TBT_R2D	PCIE_80D	PCIE_PCH_TX	PCIE TBT_R2D_N<3..0>	33
PCIE_TBT_R2D	PCIE_80D	PCIE_PCH_TX	PCIE TBT_R2D_C_P<3..0>	8 33
PCIE_TBT_R2D	PCIE_80D	PCIE_PCH_TX	PCIE TBT_R2D_C_N<3..0>	8 33
PCIE_TBT_D2R	PCIE_80D	PCIE_PCH_RX	PCIE TBT_D2R_P<3..0>	8 33
PCIE_TBT_D2R	PCIE_80D	PCIE_PCH_RX	PCIE TBT_D2R_N<3..0>	8 33
PCIE_TBT_D2R	PCIE_80D	PCIE_PCH_RX	PCIE TBT_D2R_C_P<3..0>	33
PCIE_TBT_D2R	PCIE_80D	PCIE_PCH_RX	PCIE TBT_D2R_C_N<3..0>	33
PCIE_CLK100M_TBT	CLK_PCIE_80D	CLK_PCIE	PCIE CLK100M_TBT_P	16 33
PCIE_CLK100M_TBT	CLK_PCIE_80D	CLK_PCIE	PCIE CLK100M_TBT_N	16 33
XDP_TDI	CLK_PCIE_80D	CLK_PCIE	PEG CLK100M_P	6 16
XDP_TDO	CLK_PCIE_80D	CLK_PCIE	PEG CLK100M_N	6 16
XDP_TMS	BCH_45S	BCH_ITP	XDP_PCH_TDI	16 23
XDP_TMS	BCH_45S	BCH_ITP	XDP_PCH_TDO	16 23
XDP_TCK	BCH_45S	BCH_ITP	XDP_PCH_TMS	16 23
XDP_TCK	BCH_45S	BCH_ITP	XDP_PCH_TCK	16 23

## Chipset Net Properties

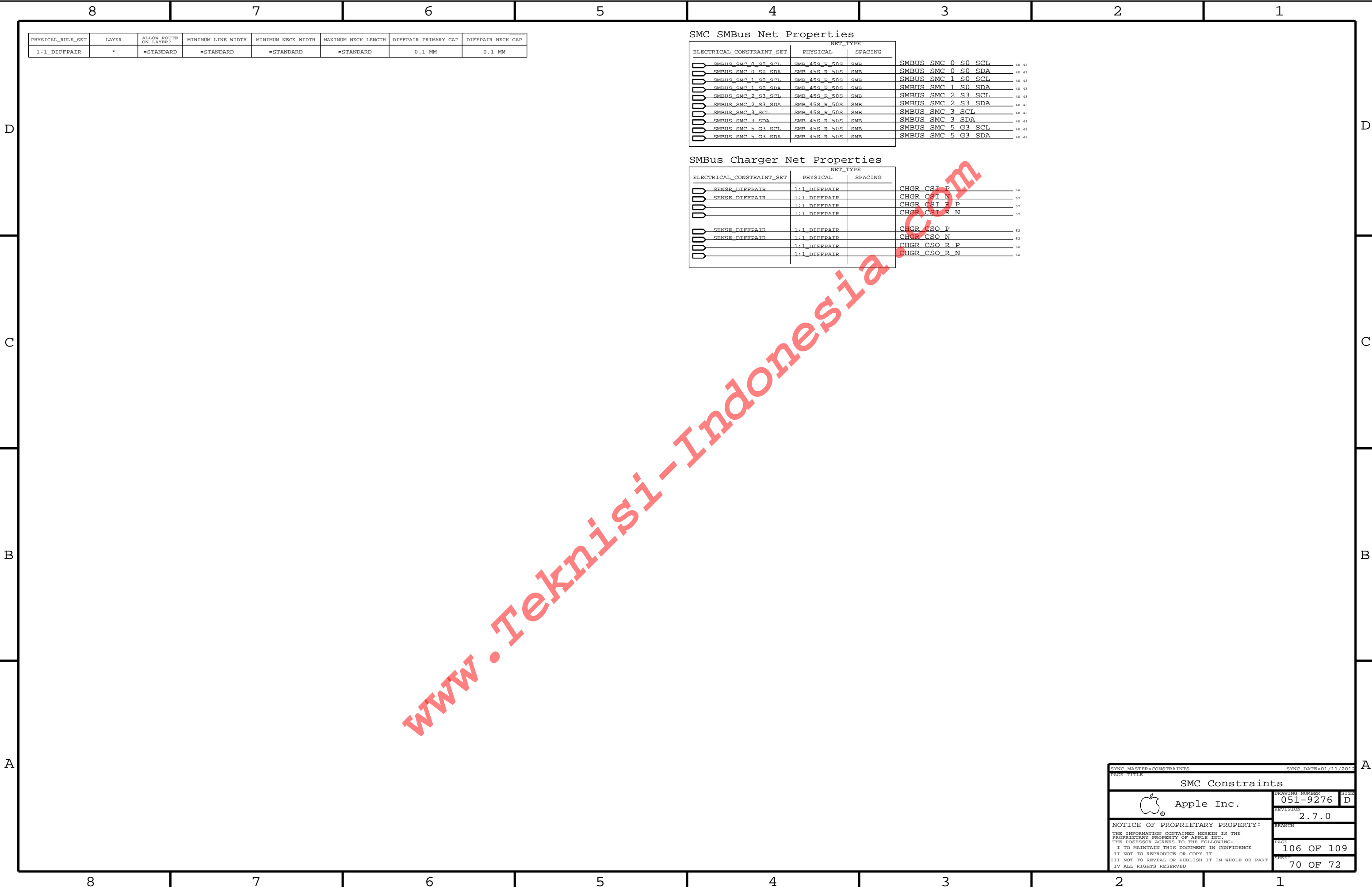
ELECTRICAL_CONSTRAINT_SET		NET_TYPE			
		PHYSICAL	SPACING		
	DP_TBT_ML	DP_80D	DP_TX	DP TBTSNK0 ML P<3...0>	33
	DP_TBT_ML	DP_80D	DP_TX	DP TBTSNK0 ML N<3...0>	33
		DP_80D	DP_TX	DP TBTSNK0 ML C P<3...0>	33
		DP_80D	DP_TX	DP TBTSNK0 ML C N<3...0>	33
	DP_TBT_AUXCH	DP_80D	DP_AUX	DP TBTSNK0 AUXCH P	33
	DP_TBT_AUXCH	DP_80D	DP_AUX	DP TBTSNK0 AUXCH N	33
		DP_80D	DP_AUX	DP TBTSNK0 AUXCH C P	33
		DP_80D	DP_AUX	DP TBTSNK0 AUXCH C N	33
	DP_TBT_ML	DP_80D	DP_TX	DP TBTSNK1 ML P<3...0>	33
	DP_TBT_ML	DP_80D	DP_TX	DP TBTSNK1 ML N<3...0>	33
		DP_80D	DP_TX	DP TBTSNK1 ML C P<3...0>	33
		DP_80D	DP_TX	DP TBTSNK1 ML C N<3...0>	33
	DP_TBT_AUXCH	DP_80D	DP_AUX	DP TBTSNK1 AUXCH P	33
	DP_TBT_AUXCH	DP_80D	DP_AUX	DP TBTSNK1 AUXCH N	33
		DP_80D	DP_AUX	DP TBTSNK1 AUXCH C P	33
		DP_80D	DP_AUX	DP TBTSNK1 AUXCH C N	33

## Clock Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE			
		PHYSICAL	SPACING		
	SYSCLK_CLK32K_RTC	CLK_SLOW_45S	CLK_SLOW	SYSCLK_CLK32K_RTC	16 25
	SYSCLK_CLK25M_SB	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_SB	16 25
		CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_SB_R	16
	SYSCLK_CLK25M_TBT	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT	25 33
		CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT_R	33
	SYSCLK_CLK25M_XTAL	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X1	25
		CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X2	25
		CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X2_R	25







PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		PHYSICAL	SPACING	
	SMBUS_SMC_0_S0_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_0_S0_SCL 40 43
	SMBUS_SMC_0_S0_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_0_S0_SDA 40 43
	SMBUS_SMC_1_S0_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_1_S0_SCL 40 43
	SMBUS_SMC_1_S0_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_1_S0_SDA 40 43
	SMBUS_SMC_2_S3_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_2_S3_SCL 40 43
	SMBUS_SMC_2_S3_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_2_S3_SDA 40 43
	SMBUS_SMC_3_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_3_SCL 40 43
	SMBUS_SMC_3_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_3_SDA 40 43
	SMBUS_SMC_5_G3_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_5_G3_SCL 40 43
	SMBUS_SMC_5_G3_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_5_G3_SDA 40 43

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		PHYSICAL	SPACING	
	SENSE_DIFFPAIR	1:1_DIFFPAIR		CHGR_CSI_P 52
	SENSE_DIFFPAIR	1:1_DIFFPAIR		CHGR_CSI_N 52
		1:1_DIFFPAIR		CHGR_CSI_R_P 52
		1:1_DIFFPAIR		CHGR_CSI_R_N 52
	SENSE_DIFFPAIR	1:1_DIFFPAIR		CHGR_CSO_P 52
	SENSE_DIFFPAIR	1:1_DIFFPAIR		CHGR_CSO_N 52
		1:1_DIFFPAIR		CHGR_CSO_R_P 52
		1:1_DIFFPAIR		CHGR_CSO_R_N 52

SYNC\_MASTER=CONSTRAINTS

SYNC\_DATE=01/11/2012

SMC Constraints

Apple Inc.

DRAWING NUMBER051-9276

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PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM_LINE_WIDTH	MINIMUM_NECK_WIDTH	MAXIMUM_NECK_LENGTH	DIFFPAIR_PRIMARY_GAP	DIFFPAIR_NECK_GAP
SENSE_1T01_45S	*	=1:1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
SENSE_1T01_P2MM	*	=1:1_DIFFPAIR	0.200 MM	0.100 MM	=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1T01_45S	*	=1:1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
SPKR_DIFFPAIR	*	=1:1_DIFFPAIR	0.300 MM	0.100 MM	=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?
AUDIO	*	=2:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
GND	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	CLK_PCIE	*	GND_P2MM
GND	PCIE*	*	GND_P2MM
GND	SATA*	*	GND_P2MM
GND	USB*	*	GND_P2MM
GND	LVDS*	*	GND_P2MM
SB_POWER	CLK_PCIE	*	PWR_P2MM
SB_POWER	SATA*	*	PWR_P2MM
SB_POWER	SATA*	*	PWR_P2MM

J11/J13 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
	SENSE_DIFFPAIR	THERM_1T01_45S	THERM	INLET THMSNS D1 P 45 46
	SENSE_DIFFPAIR	THERM_1T01_45S	THERM	INLET THMSNS D1 N 45 46
	SENSE_DIFFPAIR	THERM_1T01_45S	THERM	TBT THERMD P 46
	SENSE_DIFFPAIR	THERM_1T01_45S	THERM	TBT THERMD N 46
	SENSE_DIFFPAIR	THERM_1T01_45S	THERM	TBT MLBBOT THMSNS P 46
	SENSE_DIFFPAIR	THERM_1T01_45S	THERM	TBT MLBBOT THMSNS N 46
	SENSE_DIFFPAIR	THERM_1T01_45S	THERM	TBTTHMSNS D2 R P 46
	SENSE_DIFFPAIR	THERM_1T01_45S	THERM	TBTTHMSNS D2 R N 46
	SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	CPU THERMD P 9 46
	SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	CPU THERMD N 9 46
	SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	CPUTHMSNS D2 P 46
	SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	CPUTHMSNS D2 N 46
	SENSE_DIFFPAIR	SENSE_1T01_P2MM	SENSE	CPUVCCIOS0 CS N 44 58
	SENSE_DIFFPAIR	SENSE_1T01_P2MM	SENSE	CPUVCCIOS0 CS P 44 58
	SENSE_DIFFPAIR	SENSE_1T01_P2MM	SENSE	CPUIMVP ISNS1 P 44 56 57
	SENSE_DIFFPAIR	SENSE_1T01_P2MM	SENSE	CPUIMVP ISNS1 N 44 57
	SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	CPUIMVP ISUM R P 44
	SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	CPUIMVP ISUM R N 44
	SENSE_DIFFPAIR	SENSE_1T01_P2MM	SENSE	CPUIMVP ISNS1G P 44 57
	SENSE_DIFFPAIR	SENSE_1T01_P2MM	SENSE	CPUIMVP ISNS1G N 44 57
	SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	CPUIMVP ISUMG R P 44
	SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	CPUIMVP ISUMG R N 44
	SENSE_DIFFPAIR	SENSE_1T01_P2MM	SENSE	VCCSAS0 CS P 44 53
	SENSE_DIFFPAIR	SENSE_1T01_P2MM	SENSE	VCCSAS0 CS N 44 53
	SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	VCCSAISNS R P 44
	SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	VCCSAISNS R N 44
	SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS 3V3S0 P 44 60
	SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS 3V3S0 N 44 60
	SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS 3V3S0 R P 44
	SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS 3V3S0 R N 44
	SENSE_DIFFPAIR	SENSE_1T01_P2MM	SENSE	CPUIMVP ISUMG P 56 57
	SENSE_DIFFPAIR	SENSE_1T01_P2MM	SENSE	CPUIMVP ISUMG N 56 57
	SENSE_DIFFPAIR	SENSE_1T01_P2MM	SENSE	CPUIMVP ISUM P 56 57
	SENSE_DIFFPAIR	SENSE_1T01_P2MM	SENSE	CPUIMVP ISUM N 56 57
	SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS HS COMPUTING N 8 45
	SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS HS COMPUTING P 8 45
	SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS HS OTHER N 45
	SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS HS OTHER P 45
	SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS 1V5 S3 N 45 55
	SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS 1V5 S3 P 45 55
	SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS AIRPORT N 36 45
	SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS AIRPORT P 36 45
	SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS SSD N 37 45
	SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS SSD P 37 45
	SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS LCDBKLT N 8 45
	SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS LCDBKLT P 8 45
	AUD_DIFF	1:1_DIFFPAIR	AUDIO	SPKRAMP INR P 6 39 50
	AUD_DIFF	1:1_DIFFPAIR	AUDIO	SPKRAMP INR N 6 39 50
	SPKR_OUT	1:1_DIFFPAIR	AUDIO	MAX98300 R P 50
	SPKR_OUT	1:1_DIFFPAIR	AUDIO	MAX98300 R N 50
	SPKR_OUT	SPKR_DIFFPAIR	AUDIO	SPKRAMP ROUT P 6 50 51
	SPKR_OUT	SPKR_DIFFPAIR	AUDIO	SPKRAMP ROUT N 6 50 51
	SB_POWER		SB_POWER	PP3V3 S5 6 7
	SB_POWER		SB_POWER	PP3V3 S0 6 7
			GND	GND

## J11/J13 Board-Specific Spacing & Physical Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM	NO_TYPE, BGA	MM	16.2

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	TOP, BOTTOM	Y	=50_OHM_SE	=50_OHM_SE			
DEFAULT	ISL2, ISL11	Y	=45_OHM_SE	=45_OHM_SE			
DEFAULT	ISL3, ISL10	Y	=45_OHM_SE	=45_OHM_SE			
DEFAULT	ISL4, ISL9	Y	=45_OHM_SE	=45_OHM_SE			
DEFAULT	*	N	100 MM	100 MM	10 MM	0 MM	0 MM
STANDARD	*	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT

## Single-ended Physical Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYERS	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.310 MM	0.310 MM			
27P4_OHM_SE	ISL2,ISL11	Y	0.182 MM	0.182 MM			
27P4_OHM_SE	ISL3,ISL10	Y	0.182 MM	0.182 MM			
27P4_OHM_SE	ISL4,ISL9	Y	0.182 MM	0.182 MM			
27P4_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
35_OHM_SE	TOP,BOTTOM	Y	0.195 MM	0.195 MM			
35_OHM_SE	ISL2,ISL11	Y	0.125 MM	0.125 MM			
35_OHM_SE	ISL3,ISL10	Y	0.125 MM	0.125 MM			
35_OHM_SE	ISL4,ISL9	Y	0.125 MM	0.125 MM			
35_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.170 MM	0.170 MM			
40_OHM_SE	ISL2,ISL11	Y	0.096 MM	0.096 MM			
40_OHM_SE	ISL3,ISL10	Y	0.096 MM	0.096 MM			
40_OHM_SE	ISL4,ISL9	Y	0.099 MM	0.099 MM			
40_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP,BOTTOM	Y	0.135 MM	0.135 MM			
45_OHM_SE	ISL2,ISL11	Y	0.075 MM	0.075 MM			
45_OHM_SE	ISL3,ISL10	Y	0.075 MM	0.075 MM			
45_OHM_SE	ISL4,ISL9	Y	0.080 MM	0.080 MM			
45_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.110 MM	0.110 MM			
50_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

## Differential Pair Physical Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
72_OHM_DIFF	TOP,BOTTOM	Y	0.165 MM	0.165 MM		0.130 MM	0.130 MM
72_OHM_DIFF	ISL2,ISL11	Y	0.109 MM	0.109 MM		0.150 MM	0.150 MM
72_OHM_DIFF	ISL3,ISL10	Y	0.109 MM	0.109 MM		0.150 MM	0.150 MM
72_OHM_DIFF	ISL4,ISL9	Y	0.114 MM	0.114 MM		0.150 MM	0.150 MM
72_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	TOP,BOTTOM	Y	0.132 MM	0.132 MM		0.130 MM	0.130 MM
80_OHM_DIFF	ISL2,ISL11	Y	0.081 MM	0.081 MM		0.115 MM	0.115 MM
80_OHM_DIFF	ISL3,ISL10	Y	0.081 MM	0.081 MM		0.115 MM	0.115 MM
80_OHM_DIFF	ISL4,ISL9	Y	0.088 MM	0.088 MM		0.110 MM	0.110 MM
80_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

## Spacing Constraints

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	*	0.100 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1x_DIELECTRIC	TOP,BOTTOM	0.071 MM	?
1x_DIELECTRIC	ISL3, ISL10	0.053 MM	?
1x_DIELECTRIC	ISL4, ISL9	0.050 MM	?
1x_DIELECTRIC	*	0.090 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P2MM
CLK_P01E	*	BGA	BGA_P2MM
CLK_SLOW	*	BGA	BGA_P2MM